

SIGNAL INTEGRITY AND ELECTROMAGNETIC BROADBAND PACKAGING MODEL EXTRACTION OF FULL DIFFERENTIAL BANDPASS FILTER ON IPD WITH BGA PACKAGING

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Abstract—Since the system-level package was proposed, the electronics industry has increasingly attached importance to both directly relevant and related issues, and the scope of system-level package usage has increased. Creating more complex system-level package structures, thereby leading to the design of overall electrical effects, requires more electromagnetic simulation resources, and therefore a great deal of time in the design process. The main purpose of this paper is to analyze the effects of system-level packaging, and to establish systems-in-package in accordance with electrical specifications. Using a segmented approach, this paper also builds an overall model for designers to predict electrical characteristics, thus shortening the product development schedule. In this paper, the transmission effects of a substrate are analyzed by changing the length of the substrate transmission line, with or without a thermal ground ball and ground ring. Previously established package IP are cascaded to establish the model of the package substrate, which verifies the feasibility of the package IP. We then analyze the characteristics of the interference between chips and package using an integrated passive device, and propose a complete package equivalent circuit model.

1. INTRODUCTION

As shown in Fig. 1 [1–13], Moore's Law proposed that the number of transistors on an integrated circuit would double every 24 months (in 1975 this was changed to 18 months), enabling more chip functions

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research and technology developments each chapter has been contributed by some of the world's leading scientists and experts from academia research institutes and industry from around the globe Covers chip wafer level 3D integration technology memory stacking reconfigurable 3D and monolithic 3D IC Discusses the use of silicon interposer and organic interposer Presents architecture design and technology implementations for 3D FPGA integration Describes oxide bonding Cu SiO₂ hybrid bonding adhesive bonding and solder bonding Addresses the issue of thermal dissipation in 3D integration

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Advances in Electronic Packaging, 2001 *EDN*, 2005 **Electronic Design**, 1996 **System on Package** Rao

Tummala,2007-07-22 System on Package SOP is an emerging microelectronic technology that places an entire system on a single chip size package Where systems used to be bulky boxes housing hundreds of components SOP saves interconnection time and heat generation by keep a full system with computing communications and consumer functions all in a single chip Written by the Georgia Tech developers of the technology this book explains the basic parameters design functions and manufacturing issues showing electronic designers how this radical new packaging technology can be used to solve pressing electronics design challenges

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