

time, power dissipation, and power density are affected in terms of the scaling factor, S . To be more specific, what would happen if the design rules change from, say, $1\text{ }\mu\text{m}$ to $1/S\text{ }\mu\text{m}$ ($S>1$)?

SOLUTION :

	<i>Const E field</i>	<i>Const V_{DD}</i>
W, L, t_{ox}	$1/S$	$1/S$
V_{DD}	$1/S$	1
C_{ox}	S	S
$C = C_{ox}WL$	$1/S$	$1/S$
k_n, k_p	S	S
I_{DD}	$1/S$	S
$t_{delay} = CY/I_{DD}$	$1/S$	$1/S^2$
<i>Power</i> $I_{DD}V_{DD}$	$1/S^2$	S
<i>Power density</i> $\frac{\text{Power}}{\text{Area}}$	1	S^3

3.9 A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 110^{16}\text{ cm}^{-3}$, gate doping density (n-type poly) of $N_D = 10^{20}\text{ cm}^{-3}$, $Q_{ox} = 1/q = 4 \times 10^{10}\text{ cm}^{-2}$, and gate oxide thickness of $t_{ox} = 1.6\text{ }\mu\text{m}$. Calculate the threshold voltage at room temperature for $V_{DD}=0$. Use $\phi_s = 11.7\text{ }\mu\text{V}$.

SOLUTION :

$$\phi_{(substrate)} = \frac{kT}{q} \ln \frac{N_D}{n_i} = 0.026 \ln \frac{110^{16}}{1.45 \times 10^{10}} = 0.348[\text{V}]$$

$$\phi_{(gate)} = \frac{kT}{q} \ln \frac{N_{D,poly}}{n_i} = 0.026 \ln \frac{10^{20}}{1.45 \times 10^{10}} = 0.587[\text{V}]$$

$$\phi_{sc} = \phi_{(substrate)} - \phi_{(gate)} = 0.348 - 0.587 = -0.239[\text{V}]$$

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AW Chickering



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