

Andrei Pavlov
Manoj Sachdev

CMOS SRAM

Circuit Design and
Parametric Test in
Nano-Scaled Technologies

Process-Aware SRAM Design
and Test

Cmos Sram Circuit Design Parametric Test Amamco

Hsiao-Hsuan Liu, Francky Catthoor



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CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies Andrei Pavlov,Manoj Sachdev,2008-06-01

The monograph will be dedicated to SRAM memory design and test issues in nano scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues Purpose provide process aware solutions for SRAM design and test challenges **Process-Aware Sram Design and Test** Sherry

Andrews,2014-12-18 Nanotechnology nanotech is the manipulation of matter on an atomic molecular and supramolecular scale The earliest widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products also now referred to as molecular nanotechnology A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers This definition reflects the fact that quantum mechanical effects are important at this quantum realm scale and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold It is therefore common to see the plural form nanotechnologies as well as nanoscale technologies to refer to the broad range of research and applications whose common trait is size Because of the variety of potential applications including industrial and military governments have invested billions of dollars in nanotechnology research Through its National Nanotechnology Initiative the USA has invested 3 7 billion dollars The European Union has invested when 1 2 billion and Japan 750 million dollars *Process-Aware SRAM Design and Test* Sherry Andrews,2014-12-18 Nanotechnology nanotech is the manipulation of matter on an atomic molecular and supramolecular scale The earliest widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products also now referred to as molecular nanotechnology A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers This definition reflects the fact that quantum mechanical effects are important at this quantum realm scale and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold It is therefore common to see the plural form nanotechnologies as well as nanoscale technologies to refer to the broad range of research and applications whose common trait is size Because of the variety of potential applications including industrial and military governments have invested billions of dollars in nanotechnology research Through its National Nanotechnology Initiative the USA has invested 3 7 billion dollars The European Union has invested when 1 2 billion and Japan 750 million dollars **CMOS Test and Evaluation** Manjul Bhushan,Mark B. Ketchen,2014-12-03 CMOS Test and Evaluation A Physical

Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products covering circuit sensitivities to MOSFET characteristics impact of silicon technology process variability applications of embedded test structures and sensors product yield and reliability over the lifetime of the product This book also covers statistical data analysis and visualization techniques test equipment and CMOS product specifications and examines product behavior over its full voltage temperature and frequency range

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits

Manoj Sachdev, Jose Pineda de Gyvez, 2010-11-10 The 2nd edition of defect oriented testing has been extensively updated New chapters on Functional Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing Similarly newer material has been incorporated in digital fault modeling and analog testing chapters The strength of Defect Oriented Testing for nano Metric CMOS VLSIs lies in its industrial relevance

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques

Microelectronic Test Structures for CMOS Technology Manjul Bhushan, Mark B. Ketchen, 2011-08-26 Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test vehicles scribe lines and CMOS products The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing In this timely volume IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements Detailed examples are presented throughout many of which are equally applicable to other microelectronic technologies as well The authors overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance

of digital CMOS technology **Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits** Manoj Sachdev, Jose Pineda de Gyvez, 2008-11-01 The 2nd edition of defect oriented testing has been extensively updated New chapters on Functional Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing Similarly newer material has been incorporated in digital fault modeling and analog testing chapters The strength of Defect Oriented Testing for nano Metric CMOS VLSIs lies in its industrial relevance **Robust SRAM Designs and Analysis** Jawar Singh, Saraju P. Mohanty, Dhiraj K. Pradhan, 2012-08-01 This book provides a guide to Static Random Access Memory SRAM bitcell design and analysis to meet the nano regime challenges for CMOS devices and emerging devices such as Tunnel FETs Since process variability is an ongoing challenge in large memory arrays this book highlights the most popular SRAM bitcell topologies benchmark circuits that mitigate variability along with exhaustive analysis Experimental simulation setups are also included which cover nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Emphasis is placed throughout the book on the various trade offs for achieving a best SRAM bitcell design Provides a complete and concise introduction to SRAM bitcell design and analysis Offers techniques to face nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Includes simulation set ups for extracting different design metrics for CMOS technology and emerging devices Emphasizes different trade offs for achieving the best possible SRAM bitcell design 6T-SRAM 1Mb Design with Test Structures and Post Silicon Validation Ankita Dosi, 2017 Static random access memories SRAM are an integral part of design systems as caches and data memories that occupy one third of design space The work presents an embedded low power SRAM on a triple well process that allows body biasing control In addition to the normal mode operation the design is embedded with Physical Unclonable Function PUF Suh07 and Sense Amplifier Test SA Test mode With PUF mode structures the fabrication and environmental mismatches in bit cells are used to generate unique identification bits These bits are fixed and known as preferred state of an SRAM bit cell The direct access test structure is a measurement unit for offset voltage analysis of sense amplifiers These designs are manufactured using a foundry bulk CMOS 55 nm low power LP process The details about SRAM bit cell and peripheral circuit design is discussed in detail for certain cases the circuit simulation analysis is performed with random variations embedded in SPICE models Further post silicon testing results are discussed for normal operation of SRAMs and the special test modes The silicon and circuit simulation results for various tests are presented Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPU require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology

nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes *Parametric Reliability of 6T-SRAM Core Cell Arrays* Stefan Drapatz,2012

CMOS Circuit Design and Test Patterns for Built-in Overcurrent Testing Gesellschaft für Mathematik und Datenverarbeitung,Heinrich Theodor Vierhaus,Lothar Muhlack,Wolfgang Meyer,Uwe Glaeser,1993 **CMOS circuit design and test patterns for built in overcurrent testing** Raúl Camposano,1993

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