

Digital Integrated Circuit Testing using Transient Signal Analysis

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Abstract

A novel approach to testing CMOS digital circuits is presented that is based on an analysis of I_{DD} switching transients on the supply rails and voltage transients at selected test points. We present simulation and hardware experiments which show distinguishable characteristics between the transient waveforms of defective and non-defective devices. These variations are shown to exist for CMOS open drain and bridging defects, located both on and off of a sensitized path.

1.0 Introduction

Transient Signal Analysis (TSA) is a new parametric testing method for digital integrated circuits. In TSA, transients in both the voltage waveforms at selected test points as well as current transients on the power supply are analyzed to determine the presence of defects. TSA exploits the fact that the power supply is globally connected to a large fraction of the transistors in a CMOS digital integrated circuit. TSA is similar to power supply current (I_{DD}) test methods in this way. Since power supply connections are unbuffered at the I/O pads, it is possible to measure the high frequency components of this signal without attenuation. Thus, the I_{DD} transients reflect the switching activity associated with the propagation of signals throughout the circuit. However, in larger circuits, the number of transistors which can simultaneously switch often makes it difficult to identify a defect using this single resource. TSA improves on defect detection capabilities of I_{DD} test strategies by additionally monitoring the voltage transients at a set of test points as well as on I_{DD} . The voltage test points are typically at or near the primary outputs of the device. By using a combination of voltage transients on test signal paths and I_{DD} transients on the power supply, TSA can provide improved defect resolution while maintaining a high degree of process insensitivity when compared with other I_{DD} -based testing methods.

In this paper, we present results from four experiments conducted on actual devices with intentionally inserted bridging and open drain defects. In order to demonstrate the sensitivity advantage of TSA over logic testing, we

have placed several bridging and open drain defects into separate versions of a test circuit and have conducted experiments using two-vector test sequences that do not generate logic errors at the test points. The results presented for the experiments show regional variations in the test point signals due to the presence of the defects.

The remainder of this paper is organized as follows. In Section 2 we present related research on device testing and the motivation for our research. Section 3 presents the results of hardware experiments conducted on devices with intentionally inserted bridging and open drain defects. Section 4 gives a summary and conclusions.

2.0 Background and Motivation

Device logic testing analyzes the logical integrity of the device by using input test vectors which are a subset of all possible stimuli. However, these subsets are generated by techniques which are based on fault models that have been shown to be inadequate to detect all forms of CMOS defects [1][2]. Parametric testing strategies [3][4], on the other hand, are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of supply current or transient response. While the algorithms for generating logic tests have been improved over time to handle more types of fault behaviors, parametric testing strategies offer intrinsically better solutions since they have been developed from the structural and electrical properties of CMOS circuits.

There are many types of parametric tests that have been proposed [5]. Recent research interest has focused primarily on three types: I_{DDQ} [6], I_{DD} [7], and delay fault testing [8][9]. I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value [10]. I_{DDQ} has been shown to be an effective diagnostic technique for CMOS bridging defects, but is of limited applicability for some types of CMOS open defects [11]. Although defect observability is significantly improved by the addition of I_{DDQ} to logic tests, I_{DDQ} is handicapped by the necessarily slow test vector application rates, the limited resolution achievable for large ICs and the restricted class of CMOS circuits to which it is applicable.

Several dynamic supply current I_{DD} -based approaches

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IC Test Using the Energy Consumption Ratio Wanli Jiang, 2000 *IEEE VLSI Test Symposium*, 2004 **18th IEEE VLSI Test Symposium**, 2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test compaction and design validation analog BIST and functional test and verification issues Also covered are STIL extension IDDQ test and on line testing and fault tolerance Lacks a subject index Annotation copyrighted by Book News Inc Portland OR Proceedings, International Test Conference 1996, 1996 ITC is the World's largest premier technical conference on the testing and total quality of integrated electronics and the assemblies and systems that are based on them *Proceedings*, 2002 *19th IEEE VLSI Test Symposium*, 2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc

Proceedings Ieee, 2004 The proceedings of the 21st IEEE VLSI test symposium VTS 2003 describing innovations in the testing of integrated circuits and systems **Asian Test Symposium**, 2004 **Digest of Technical Papers**, 2001

Test Cost Reduction Techniques Xiaoyun Sun, 2005 **Proceedings, International Test Conference 1997**, 1997

European Test Workshop 1999 Hans-Joachim Wunderlich, 1999 Annotation This proceedings contains extended version of a selected subset of the contributions presented at the May 1999 IEEE workshop The 27 papers share research and development RandD results in electronic testing Topics include calculating efficient LFSR seeds for built in self test functional and structural testing of switched current circuits compaction of IDDQ test sequence using reassignment method debug facilities in the TriMedia CPU64 architecture deterministic BIST with partial scan and using the BS register for capturing and storing n bit sequences in real time Other papers address MEMs switched capacitors ATPG and fault modeling fault simulation and fault coverage of analog circuits FPGAs and regular arrays and low power BIST No subject index Annotation copyrighted by Book News Inc Portland OR *Computer-Aided Design of Analog Integrated Circuits and Systems* Rob A. Rutenbar, Georges G. E. Gielen, 2002-05-06 The tools and techniques you need to break the analog design

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Table of Contents Digital Integrated Circuit Testing Using Transient Signal

1. Understanding the eBook Digital Integrated Circuit Testing Using Transient Signal
 - The Rise of Digital Reading Digital Integrated Circuit Testing Using Transient Signal
 - Advantages of eBooks Over Traditional Books
2. Identifying Digital Integrated Circuit Testing Using Transient Signal
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in a Digital Integrated Circuit Testing Using Transient Signal
 - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Integrated Circuit Testing Using Transient Signal
 - Personalized Recommendations
 - Digital Integrated Circuit Testing Using Transient Signal User Reviews and Ratings
 - Digital Integrated Circuit Testing Using Transient Signal and Bestseller Lists

5. Accessing Digital Integrated Circuit Testing Using Transient Signal Free and Paid eBooks
 - Digital Integrated Circuit Testing Using Transient Signal Public Domain eBooks
 - Digital Integrated Circuit Testing Using Transient Signal eBook Subscription Services
 - Digital Integrated Circuit Testing Using Transient Signal Budget-Friendly Options
6. Navigating Digital Integrated Circuit Testing Using Transient Signal eBook Formats
 - ePub, PDF, MOBI, and More
 - Digital Integrated Circuit Testing Using Transient Signal Compatibility with Devices
 - Digital Integrated Circuit Testing Using Transient Signal Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Digital Integrated Circuit Testing Using Transient Signal
 - Highlighting and Note-Taking Digital Integrated Circuit Testing Using Transient Signal
 - Interactive Elements Digital Integrated Circuit Testing Using Transient Signal
8. Staying Engaged with Digital Integrated Circuit Testing Using Transient Signal
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Integrated Circuit Testing Using Transient Signal
9. Balancing eBooks and Physical Books Digital Integrated Circuit Testing Using Transient Signal
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Digital Integrated Circuit Testing Using Transient Signal
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Digital Integrated Circuit Testing Using Transient Signal
 - Setting Reading Goals Digital Integrated Circuit Testing Using Transient Signal
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Digital Integrated Circuit Testing Using Transient Signal
 - Fact-Checking eBook Content of Digital Integrated Circuit Testing Using Transient Signal
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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