

1 10g 25g High Speed Ethernet Subsystem V2 Xilinx

**Marco Gottardo, Phd Marco Gottardo
Ing**

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FPGA to High Speed Adc Data Streaming, Hdl Programming Marco Gottardo, Phd Marco Gottardo Ing, 2018-06-06 The book set the objective to design and test a high speed and high density data acquisition system based on the latest generation FPGA technologies. Topic is from the author Phd thesis and shows the latest products released by Xilinx to design an acquire stream system of signals from generic probes specifically magnetic probes applied on a nuclear fusion experiment located in Padova Italy. The Zynq 7000 family is nowadays state of the art of system SoC that integrates a powerful and extensive FPGA section with an ARM multicore with the architecture Cortex A9. Inside the book the basis of HDL programming on Vivado IDE.

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