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CMOS SRAM

Circuit Design and
Parametric Test in
Nano-Scaled Technologies

Process-Aware SRAM Design
and Test

Cmos Sram Circuit Design And Parametric Test In Nano Scaled Technologies Process Aware Sram Design And Test Frontiers In Electronic Testing

Manoj Sachdev, Jose Pineda de Gyvez



Cmos Sram Circuit Design And Parametric Test In Nano Scaled Technologies Process Aware Sram Design And Test Frontiers In Electronic Testing:

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies Andrei Pavlov,Manoj Sachdev,2008-06-01 The monograph will be dedicated to SRAM memory design and test issues in nano scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues Purpose provide process aware solutions for SRAM design and test challenges

VLSI, Communication and Signal Processing R. K. Nagaria,V. S. Tripathi,Carlos Ruiz Zamarreno,Yogendra Kumar Prajapati,2023-07-01 This book covers a variety of topics in Electronics and Communication Engineering especially in the area of microelectronics and VLSI design communication systems and networks and signal and image processing The content is based on papers presented at the 5th International Conference on VLSI Communication and Signal Processing VCAS 2022 The book also discusses the emerging applications of novel tools and techniques in image video and multimedia signal processing This book is useful to students researchers and professionals working in the electronics and communication domain

Process-Aware Sram Design and Test Sherry Andrews,2014-12-18 Nanotechnology nanotech is the manipulation of matter on an atomic molecular and supramolecular scale The earliest widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products also now referred to as molecular nanotechnology A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers This definition reflects the fact that quantum mechanical effects are important at this quantum realm scale and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold It is therefore common to see the plural form nanotechnologies as well as nanoscale technologies to refer to the broad range of research and applications whose common trait is size Because of the variety of potential applications including industrial and military governments have invested billions of dollars in nanotechnology research Through its National Nanotechnology Initiative the USA has invested 3 7 billion dollars The European Union has invested when 1 2 billion and Japan 750 million dollars

Process-Aware SRAM Design and Test Sherry Andrews,2014-12-18 Nanotechnology nanotech is the manipulation of matter on an atomic molecular and supramolecular scale The earliest widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products also now referred to as molecular nanotechnology A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers This definition reflects the fact that quantum mechanical effects are important at this quantum

realm scale and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold It is therefore common to see the plural form nanotechnologies as well as nanoscale technologies to refer to the broad range of research and applications whose common trait is size Because of the variety of potential applications including industrial and military governments have invested billions of dollars in nanotechnology research Through its National Nanotechnology Initiative the USA has invested 3.7 billion dollars The European Union has invested when 1.2 billion and Japan 750 million dollars

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, Jose Pineda de Gyvez, 2008-11-01 The 2nd edition of defect oriented testing has been extensively updated New chapters on Functional Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing Similarly newer material has been incorporated in digital fault modeling and analog testing chapters The strength of Defect Oriented Testing for nano Metric CMOS VLSIs lies in its industrial relevance

Robust Optimization of Nanometer SRAM Designs Akshit Dayal, 2011 Technology scaling has been the most obvious choice of designers and chip manufacturing companies to improve the performance of analog and digital circuits With the ever shrinking technological node process variations can no longer be ignored and play a significant role in determining the performance of nanoscaled devices By choosing a worst case design methodology circuit designers have been very munificent with the design parameters chosen often manifesting in pessimistic designs with significant area overheads Significant work has been done in estimating the impact of intra die process variations on circuit performance pertinently

noise margin and standby leakage power for fixed transistor channel dimensions. However, for an optimal high yield SRAM cell design, it is absolutely imperative to analyze the impact of process variations at every design point, especially since the distribution of process variations is a statistically varying parameter and has an inverse correlation with the area of the MOS transistor. Furthermore, the first order analytical models used for optimization of SRAM memories are not as accurate, and the impact of voltage and its inclusion as an input along with other design parameters is often ignored. In this thesis, the performance parameters of a nano scaled 6 T SRAM cell are modeled as an accurate yield aware empirical polynomial predictor in the presence of intra die process variations. The estimated empirical models are used in a constrained non linear robust optimization framework to design an SRAM cell for a 45 nm CMOS technology having optimal performance according to bounds specified for the circuit performance parameters with the objective of minimizing on chip area. This statistically aware technique provides a more realistic design methodology to study the trade off between performance parameters of the SRAM. Furthermore, a dual optimization approach is followed by considering SRAM power supply and wordline voltages as additional input parameters to simultaneously tune the design parameters ensuring a high yield and considerable area reduction. In addition, the cell level optimization framework is extended to the system level optimization of caches under both cell level and system level performance constraints.

Modeling, Optimization and Testing for Analog/mixed-signal Circuits in Deeply Scaled CMOS Technologies Guo Yu, 2011. As CMOS technologies move to sub 100nm regions, the design and verification for analog mixed signal circuits become more and more difficult due to the problems including the decrease of transconductance, severe gate leakage and profound mismatches. The increasing manufacturing induced process variations and their impacts on circuit performances make the already complex circuit design even more sophisticated in the deeply scaled CMOS technologies. Given these barriers, efforts are needed to ensure the circuits are robust and optimized with consideration of parametric variations. This research presents innovative computer aided design approaches to address three such problems: 1) large analog mixed signal performance modeling under process variations, 2) yield aware optimization for complex analog mixed signal systems, and 3) on chip test scheme development to detect and compensate parametric failures. The first problem focuses on the efficient circuit performance evaluation with consideration of process variations, which serves as the baseline for robust analog circuit design. We propose statistical performance modeling methods for two popular types of complex analog mixed signal circuits including Sigma Delta ADCs and charge pump PLLs. A more general performance modeling is achieved by employing a geostatistics motivated performance model, Kriging model, which is accurate and efficient for capturing stand alone analog circuit block performances. Based on the generated block level performance models, we can solve the more challenging problem of yield aware system optimization for large analog mixed signal systems. Multi yield pareto fronts are utilized in the hierarchical optimization framework so that the statistical optimal solutions can be achieved efficiently for the systems. We further look into on chip design for test DFT circuits in analog

systems and solve the problems of linearity test in ADCs and DFT scheme optimization in charge pump PLLs Finally a design example of digital intensive PLL is presented to illustrate the practical applications of the modeling optimization and testing approaches for large analog mixed signal systems

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions

Variation-Aware Advanced CMOS Devices and SRAM Changhwan Shin, 2016-06-06 This book provides a comprehensive overview of contemporary issues in complementary metal oxide semiconductor CMOS device design describing how to overcome process induced random variations such as line edge roughness random dopant fluctuation and work function

variation and the applications of novel CMOS devices to cache memory or Static Random Access Memory SRAM The author places emphasis on the physical understanding of process induced random variation as well as the introduction of novel CMOS device structures and their application to SRAM The book outlines the technical predicament facing state of the art CMOS technology development due to the effect of ever increasing process induced random intrinsic variation in transistor performance at the sub 30 nm technology nodes Therefore the physical understanding of process induced random intrinsic variations and the technical solutions to address these issues plays a key role in new CMOS technology development This book aims to provide the reader with a deep understanding of the major random variation sources and the characterization of each random variation source Furthermore the book presents various CMOS device designs to surmount the random variation in future CMOS technology emphasizing the applications to SRAM

Circuit-Technology Co-Optimization of SRAM Design in Advanced CMOS Nodes Hsiao-Hsuan Liu, Francky Catthoor, 2024-12-20 Modern computing engines CPUs GPUs and NPUs require extensive SRAM for cache designs driven by the increasing demand for higher density performance and energy efficiency This book delves into two primary areas within ultra scaled technology nodes 1 advancing SRAM bitcell scaling and 2 exploring innovative subarray designs to enhance power performance area PPA metrics across technology nodes The first part of the book utilizes a bottom up design technology co optimization DTCO approach employing a dedicated PPA simulation framework to evaluate and identify the most promising strategies for SRAM bitcell scaling It offers a comprehensive examination of SRAM bitcell scaling beyond 1 nm node outlining a structured research cycle that includes identifying scaling bottlenecks developing cutting edge architectures with complementary field effect transistor CFET technology and addressing challenges such as process integration and routing complexities Additionally this book introduces a novel write margin methodology to better address the risks of write failures in resistance dominated nodes This methodology accounts for time dependent parasitic bitline effects and incorporates timing setup of write assist techniques to prevent underestimating the yield loss In the second part the focus shifts to a top down DTCO approach due to the diminishing returns of bitcell scaling beyond 5 node at the macro level As technology scales increasing resistance and capacitance RC lead designers to adopt smaller subarray sizes to reduce effective RC and enhance subarray level PPA However this approach can result in increased inter subarray interconnect overhead potentially offsetting macro level improvements This book examines the effects of various subarray sizes on macro level PPA and finds that larger subarrays can significantly reduce interconnect overhead and improve the energy delay area product EDAP of SRAM macro The introduction of the active interconnect AIC concept enables the use of larger subarray sizes while integrating carbon nanotube FET as back end of line compatible devices results in macro level EDAP improvements of up to 65% when transitioning from standard subarrays to AIC divided subarrays These findings highlight the future trajectory of SRAM subarray design in deeply scaled nodes

Low-power, Low-voltage SRAM Circuits Design for Nanometric CMOS

Technologies Tahseen Shakir, 2011 Embedded SRAM memory is a vital component in modern SoCs. More than 80% of the System on Chip (SoC) die area is often occupied by SRAM arrays. As such, system reliability and yield is largely governed by the SRAM's performance and robustness. The aggressive scaling trend in CMOS device minimum feature size coupled with the growing demand in high capacity memory integration has imposed the use of minimal size devices to realize a memory bitcell. The smallest 6T SRAM bitcell to date occupies a $0.1 \mu\text{m}^2$ in silicon area. SRAM bitcells continue to benefit from an aggressive scaling trend in CMOS technologies. Unfortunately, other system components such as interconnects experience a slower scaling trend. This has resulted in dramatic deterioration in a cell's ability to drive a heavily loaded interconnect. Moreover, the growing fluctuation in device properties due to Process Voltage and Temperature (PVT) variations has added more uncertainty to SRAM operation. Thus, ensuring the ability of a miniaturized cell to drive heavily loaded bitlines and to generate adequate voltage swing is becoming challenging. A large percentage of state-of-the-art SoC system failures are attributed to the inability of SRAM cells to generate the targeted bitline voltage swing within a given access time. The use of read assist mechanisms and current mode sense amplifiers are the two key strategies used to surmount bitline loading effects. On the other hand, new bitcell topologies and cell supply voltage management are used to overcome fluctuations in device properties. In this research, we tackled conventional 6T SRAM bitcell limited drivability by introducing new integrated voltage sensing schemes and current mode sense amplifiers. The proposed schemes feature a read assist mechanism. The proposed schemes' functionality and superiority over existing schemes are verified using transient and statistical SPICE simulations. Post-layout extracted views of the devices are used for realistic simulation results. Low voltage operated SRAM reliability and yield enhancement is investigated, and a wordline boost technique is proposed as a means to manage the cell's WL operating voltage. The proposed wordline driver design shows a significant improvement in reliability and yield in a 400 mV 6T SRAM cell. The proposed wordline driver design exploits the cell's Dynamic Noise Margin (DNM) to boost peak level and boost decay rate. Programmability features are added. SPICE transient and statistical simulations are used to verify the proposed design's functionality. Finally, at a bitcell level, we proposed a new five-transistor 5T SRAM bitcell which shows competitive performance and reliability figures of merit compared to the conventional 6T bitcell. The functionality of the proposed cell is verified by post-layout SPICE simulations. The proposed bitcell topology is designed, implemented, and fabricated in a standard ST CMOS 65nm technology process. A $1.2 \times 1.2 \text{ mm}^2$ multi-design project test chip consisting of four 32 Kbit $256 \text{ row} \times 128 \text{ column}$ SRAM macros with the required peripheral and timing control units is fabricated. Two of the designed SRAM macros are dedicated for this work, namely a 32 Kbit 5T macro and a 32 Kbit 6T macro, which is used as a comparison reference. Other macros belong to other projects and are not discussed in this document.

Robust SRAM Designs and Analysis Jawar Singh, Saraju P. Mohanty, Dhiraj K. Pradhan, 2012-08-01 This book provides a guide to Static Random Access Memory (SRAM) bitcell design and analysis to meet the nano regime challenges for CMOS devices and

emerging devices such as Tunnel FETs Since process variability is an ongoing challenge in large memory arrays this book highlights the most popular SRAM bitcell topologies benchmark circuits that mitigate variability along with exhaustive analysis Experimental simulation setups are also included which cover nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Emphasis is placed throughout the book on the various trade offs for achieving a best SRAM bitcell design Provides a complete and concise introduction to SRAM bitcell design and analysis Offers techniques to face nano regime challenges such as process variation leakage and NBTI for SRAM design and analysis Includes simulation set ups for extracting different design metrics for CMOS technology and emerging devices Emphasizes different trade offs for achieving the best possible SRAM bitcell design

Nano-CMOS Design for Manufacturability Ban P. Wong, Anurag Mittal, Greg W. Starr, Franz Zach, Victor Moroz, Andrew Kahng, 2008-12-29 Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano CMOS Design for Manufacturability examines the challenges that design engineers face in the nano scaled era such as exacerbated effects and the proven design for manufacturability DFM methodology in the midst of increasing variability and design process interactions In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law the authors also tackle complex issues in the design process to overcome the difficulties including the use of a functional first silicon to support a predictable product ramp Moreover they introduce several emerging concepts including stress proximity effects contour based extraction and design process interactions This book is the sequel to Nano CMOS Circuit and Physical Design taking design to technology nodes beyond 65nm geometries It is divided into three parts Part One Newly Exacerbated Effects introduces the newly exacerbated effects that require designers attention beginning with a discussion of the lithography aspects of DFM followed by the impact of layout on transistor performance Part Two Design Solutions examines how to mitigate the impact of process effects discussing the methodology needed to make sub wavelength patterning technology work in manufacturing as well as design solutions to deal with signal power integrity WELL stress proximity effects and process variability Part Three The Road to DFM describes new tools needed to support DFM efforts including an auto correction tool capable of fixing the layout of cells with multiple optimization goals followed by a look ahead into the future of DFM Throughout the book real world examples simplify complex concepts helping readers see how they can successfully handle projects on Nano CMOS nodes It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and in short make designs that are not only functional but that also meet power and performance goals within the design schedule

Microelectronic Test Structures for CMOS Technology Manjul Bhushan, Mark B. Ketchen, 2011-08-26 Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test vehicles scribe lines and CMOS products The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased

cost and complexity of development and manufacturing In this timely volume IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements Detailed examples are presented throughout many of which are equally applicable to other microelectronic technologies as well The authors overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology *CMOS Test and Evaluation* Manjul Bhushan, Mark B. Ketchen, 2014-12-03 CMOS Test and Evaluation A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products covering circuit sensitivities to MOSFET characteristics impact of silicon technology process variability applications of embedded test structures and sensors product yield and reliability over the lifetime of the product This book also covers statistical data analysis and visualization techniques test equipment and CMOS product specifications and examines product behavior over its full voltage temperature and frequency range *Nano-scale CMOS Analog Circuits* Soumya Pandit, Chittaranjan Mandal, Amit Patra, 2018-09-03 Reliability concerns and the limitations of process technology can sometimes restrict the innovation process involved in designing nano scale analog circuits The success of nano scale analog circuit design requires repeat experimentation correct analysis of the device physics process technology and adequate use of the knowledge database Starting with the basics Nano Scale CMOS Analog Circuits Models and CAD Techniques for High Level Design introduces the essential fundamental concepts for designing analog circuits with optimal performances This book explains the links between the physics and technology of scaled MOS transistors and the design and simulation of nano scale analog circuits It also explores the development of structured computer aided design CAD techniques for architecture level and circuit level design of analog circuits The book outlines the general trends of technology scaling with respect to device geometry process parameters and supply voltage It describes models and optimization techniques as well as the compact modeling of scaled MOS transistors for VLSI circuit simulation Includes two learning based methods the artificial neural network ANN and the least squares support vector machine LS SVM method Provides case studies demonstrating the practical use of these two methods Explores circuit sizing and specification translation tasks Introduces the particle swarm optimization technique and provides examples of sizing analog circuits Discusses the advanced effects of scaled MOS transistors like narrow width effects and vertical and lateral channel engineering Nano Scale CMOS Analog Circuits Models and CAD Techniques for High Level Design describes the models and CAD techniques explores the physics of MOS transistors and considers the design challenges involving statistical variations of process technology parameters and reliability constraints related to circuit design 6T-SRAM 1Mb Design with Test Structures and Post Silicon Validation Ankita Dosi, 2017 Static random access memories SRAM are an integral part of design systems as caches and data memories that occupy one third of design space

The work presents an embedded low power SRAM on a triple well process that allows body biasing control. In addition to the normal mode operation, the design is embedded with Physical Unclonable Function (PUF) [Suh07] and Sense Amplifier Test (SAT) mode. With PUF mode structures, the fabrication and environmental mismatches in bit cells are used to generate unique identification bits. These bits are fixed and known as the preferred state of an SRAM bit cell. The direct access test structure is a measurement unit for offset voltage analysis of sense amplifiers. These designs are manufactured using a foundry bulk CMOS 55 nm low power LP process. The details about SRAM bit cell and peripheral circuit design are discussed in detail. For certain cases, the circuit simulation analysis is performed with random variations embedded in SPICE models. Further, post-silicon testing results are discussed for normal operation of SRAMs and the special test modes. The silicon and circuit simulation results for various tests are presented.

Nano-CMOS Circuit and Physical Design Ban Wong, Anurag Mittal, Yu Cao, Greg W. Starr, 2005-04-08. Based on the authors' expansive collection of notes taken over the years, *Nano CMOS Circuit and Physical Design* bridges the gap between physical and circuit design and fabrication, processing, manufacturability, and yield. This innovative book covers process technology, including sub-wavelength optical lithography, impact of process scaling on circuit and physical implementation, and low power with leaky transistors and DFM, yield, and the impact of physical implementation.

Delve into the emotional tapestry woven by in **Cmos Sram Circuit Design And Parametric Test In Nano Scaled Technologies Process Aware Sram Design And Test Frontiers In Electronic Testing** . This ebook, available for download in a PDF format (*), is more than just words on a page; it's a journey of connection and profound emotion. Immerse yourself in narratives that tug at your heartstrings. Download now to experience the pulse of each page and let your emotions run wild.

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