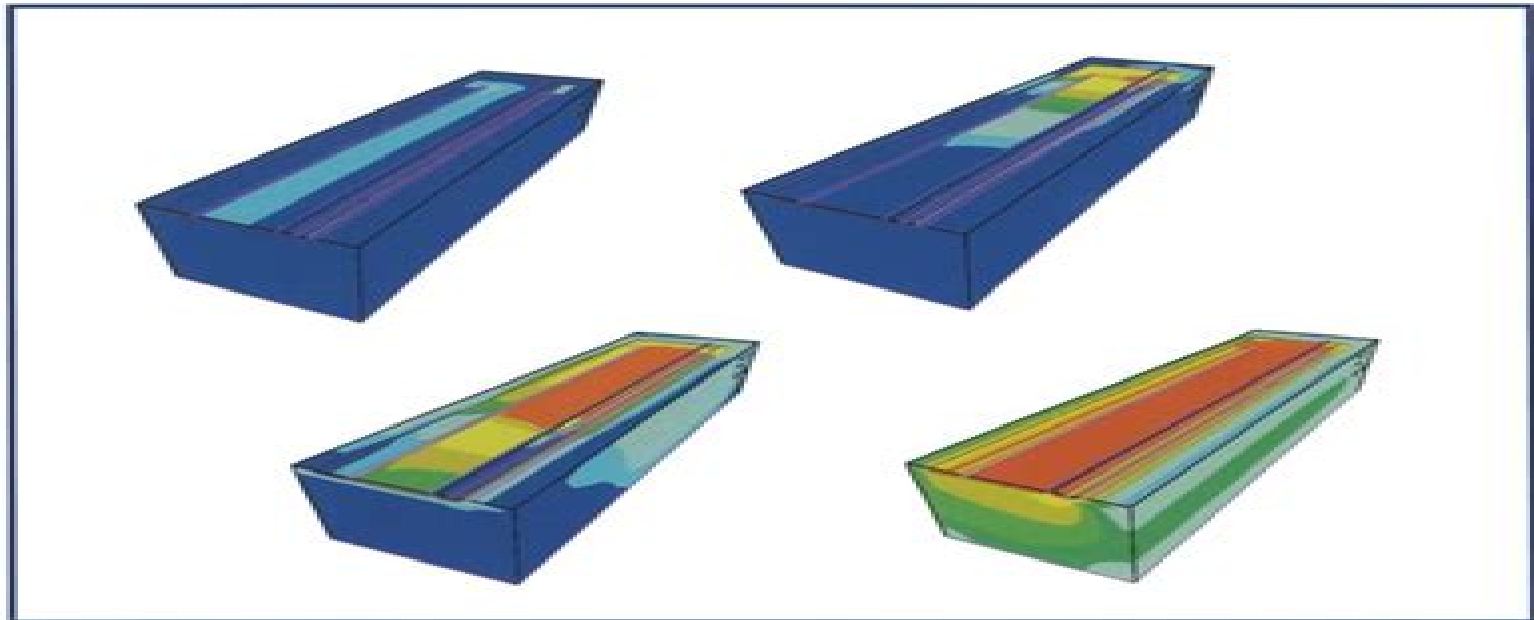


Advanced Simulation Methods for ESD Protection Development



Kai Esmark, Harald Gossner & Wolfgang Stadler

Simulation Methods For ESD Protection Development By Harald Gossner

Prasun Kumar Raha



Simulation Methods For ESD Protection Development By Harald Gossner:

Simulation Methods for ESD Protection Development Harald Gossner, Kai Esmark, Wolfgang Stadler, 2003-10-16

Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow which is now available due advances made in the field during the recent years These findings allow for an early stable ESD concept at a very early stage of the technology development which is essential now development cycles have been reduced The book also offers ways of increasing the optimization and control of the technology concerning performance thus making the process more cost effective and increasingly efficient This title provides a guide through the latest research and technology presenting the ESD protection development methodology This is based on a combination of process device and circuit stimulation and addresses the optimization of the industry critical issue reduced development cycles Written to address the needs of the ESD engineer this text is required reading by all industry practitioners and researchers and students within this field The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles and provides solutions Presents the latest research in the field with high practical relevance and its results

System Level ESD Co-Design Charvaka Duvvury, Harald Gossner, 2017-05-05 An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000 4 2 is paramount for any system design This pioneering book presents the collective knowledge of system designers and system testing experts and state of the art techniques for achieving efficient system level ESD protection with minimum impact on the system performance All categories of system failures ranging from hard to soft types are considered to review simulation and tool applications that can be used The principal focus of System Level ESD Co Design is defining and establishing the importance of co design efforts from both IC supplier and system builder perspectives ESD designers often face challenges in meeting customers system level ESD requirements and therefore a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance With contributions from Robert Ashton Jeffrey Dunnihoo Micheal Hopkins Pratik Maheshwari David Pomerence Wolfgang Reinprecht and Matti Usumaki readers benefit from hands on experience and in depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD robust systems that include mobile and automotive applications The first dedicated resource to system level ESD co design this is an essential reference for industry ESD designers system builders IC suppliers and customers and also Original Equipment Manufacturers OEMs Key features Clarifies the concept of system level ESD protection Introduces a co design approach for ESD robust systems Details soft and hard ESD fail mechanisms Detailed protection strategies for both mobile and automotive applications Explains simulation tools and methodology for system level ESD co design and overviews available test methods and standards Highlights economic benefits of system ESD co design

System Level ESD

Co-Design Charvaka Duvvury, Harald Gossner, 2015-09-08 An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000 4 2 is paramount for any system design This pioneering book presents the collective knowledge of system designers and system testing experts and state of the art techniques for achieving efficient system level ESD protection with minimum impact on the system performance All categories of system failures ranging from hard to soft types are considered to review simulation and tool applications that can be used The principal focus of System Level ESD Co Design is defining and establishing the importance of co design efforts from both IC supplier and system builder perspectives ESD designers often face challenges in meeting customers system level ESD requirements and therefore a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance With contributions from Robert Ashton Jeffrey Dunnihoo Micheal Hopkins Pratik Maheshwari David Pomerence Wolfgang Reinprecht and Matti Usumaki readers benefit from hands on experience and in depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD robust systems that include mobile and automotive applications The first dedicated resource to system level ESD co design this is an essential reference for industry ESD designers system builders IC suppliers and customers and also Original Equipment Manufacturers OEMs Key features Clarifies the concept of system level ESD protection Introduces a co design approach for ESD robust systems Details soft and hard ESD fail mechanisms Detailed protection strategies for both mobile and automotive applications Explains simulation tools and methodology for system level ESD co design and overviews available test methods and standards Highlights economic benefits of system ESD co design

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that are not well understood The endeavor of this research is to develop novel effective and robust ESD protection solutions for both emerging technologies and modern complementary metal oxide semiconductor CMOS technologies The Si nanowire field effect transistors are projected by the International Technology Roadmap for Semiconductors as promising next generation CMOS devices due to their superior DC and RF performances as well as ease of fabrication in existing Silicon processing Aiming at proposing ESD protection solutions for nanowire based circuits the dimension parameters fabrication process and layout dependency of such devices under Human Body Mode HBM ESD stresses are studied experimentally in company with failure analysis revealing the failure mechanism induced by ESD The findings including design methodologies failure mechanism and technology comparisons should provide practical knowhow of the development of ESD protection schemes for the nanowire based integrated circuits Organic thin film transistors OTFTs are the basic elements for the emerging flexible printable large area and low cost organic electronic circuits Although there are plentiful studies focusing on the DC stress induced reliability degradation the operation mechanism of OTFTs subject to ESD is not yet available in the literature and are urgently needed before the organic technology can be pushed into consumer market In this work the ESD operation mechanism of OTFT depending on gate biasing condition and dimension parameters are investigated by extensive characterization and thorough evaluation The device degradation evolution and failure mechanism under ESD are also investigated by specially designed experiments In addition to the exploration of ESD protection solutions in emerging technologies efforts have also been placed in the design and analysis of a major ESD protection device diode triggered silicon controlled rectifier DTSCR in modern CMOS technology 90nm bulk On the one hand a new type DTSCR having bi directional conduction capability optimized design window high HBM robustness and low parasitic capacitance are developed utilizing the combination of a bi directional silicon controlled rectifier and bi directional diode strings On the other hand the HBM and Charged Device Mode CDM ESD robustness of DTSCRs using four typical layout topologies are compared and analyzed in terms of trigger voltage holding voltage failure current density turn on time and overshoot voltage The advantages and drawbacks of each layout are summarized and those offering the best overall performance are suggested at the end

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