

DIGITAL HILBERT TRANSFORMERS FOR FPGA-BASED PHASE-LOCKED LOOPS

Martin Kumm, M. Shahab Sanjari

Gesellschaft für Schwerionenforschung (GSI)
64291 Darmstadt
email: m.kumm@gsi.de, s.sanjari@gsi.de

ABSTRACT

The phase detector is a main building block in phase-locked loop (PLL) applications. FPGAs permit the realtime implementation of the CORDIC algorithm which offers an efficient solution for an accurate phase detection, provided that the signal is available as an analytic signal. Different architectures for generating analytic signals by approximating the Hilbert transform were analyzed. Thereby, the focus has been on the demands based on the PLL application and the efficient implementation on FPGAs. Two methods were implemented using either FIR or complex filters. The FIR method results in a remaining phase error that has a zero mean value in time domain. An efficient IIR low-pass structure is proposed to suppress this phase error. The complex filters were implemented using a novel method based on complex, multiplier-less frequency sampling filters. Structures with different complexities are presented. A better result was achieved compared to a standard IIR filter design.

1. INTRODUCTION

Recent advances in the technology of field programmable gate arrays (FPGA) enable the implementation of all-digital phase-locked loops (ADPLL) working directly in the high frequency range, unlike traditional microprocessor-based approaches. An offset-local oscillator (Offset-LO) PLL [1] was needed within a phase measurement system for the heavy-ion synchrotron (SIS18) accelerator at GSI. This system is used to determine the phase difference of RF cavities in relation to other cavities [2] or the beamphase [3] to compensate for deviations in a closed-loop control.

PLLs are widely used in communication systems. Many specialized integrated circuits exist that suit most of these applications. Due to the requirements of this Offset-LO, an FPGA-based implementation was realized instead, which particularly covers the relatively wide frequency range ($f_{RF} = 0.8 - 5.4$ MHz) and provides a phase accuracy better than 5° during the accelerating frequency ramp ($f_{RF,max} = 68$ MHz/s).

The phase detector is a key component in a PLL. Most VLSI implementations use phase detection methods, such as

flip-flop based phase frequency detectors or time-to-digital converters, that are not feasible on FPGAs with an acceptable phase accuracy. A sophisticated way in detecting the phase is provided by the coordinate rotation digital computer (CORDIC) algorithm which was presented by Volder in 1959 and was enhanced by Walther in 1971 [4]. An existing VHDL implementation of the algorithm from Guntoro [5] could be readily used. The CORDIC algorithm implies that the input is a (complex) analytic signal, which consists of in-phase (real part) and quadrature component (imaginary part). The connection between in-phase (I) and quadrature component (Q) is given by the Hilbert transform which will be described in the next section.

Different methods exist for generating the analytic signal from a real valued signal. They are described and compared in Section 3. The implementation of a Hilbert transform with a single real FIR filter is described in Section 4. Even though modern FPGAs include hardware multipliers, these are still a limited resource in affordable devices. A novel method for designing complex multiplier-less frequency sampling filters as Hilbert transformers is presented in Section 5.

2. PHASE DETECTION WITH ANALYTIC SIGNALS

A high resolution phase detector can be realized by using the concept of the analytic signal. An analytic signal can formally be generated from a real signal by using the Hilbert transform. The discrete Hilbert transform can be formulated as a convolution with a frequency response of

$$H_H(e^{j\Omega}) = \begin{cases} -j & \text{for } 0 < \Omega < \pi \\ j & \text{for } -\pi < \Omega < 0 \\ 0 & \text{for } \Omega = 0 \end{cases} \quad (1)$$

with $\Omega = 2\pi f/f_s$, where f_s is the sampling frequency in Hz and $j = \sqrt{-1}$. The absolute amplitude is unity for all frequencies not equal to zero. The phase is -90° for all positive, and $+90^\circ$ for all negative frequencies. The inverse Fourier transform results in the impulse response

$$h_H(n) = \frac{1 - \cos(\pi n)}{\pi n} = \begin{cases} 2/(\pi n) & \text{for odd } n \\ 0 & \text{for even } n. \end{cases} \quad (2)$$

Digital Hilbert Transformers For Fpga Based Phase Locked

**Saleh R. Al-Araji,Zahir M.
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New Approaches for Multidimensional Signal Processing Lakhmi C. Jain, Rumen P. Mironov, Roumiana A. Kountcheva, Ivo Draganov, 2025-05-26 This book is a collection of papers presented at the International Workshop on New Approaches for Multidimensional Signal Processing NAMSP 2024 held at Technical University of Sofia Sofia Bulgaria during 25-27 July 2024. The book covers research papers in the field of N-dimensional multicomponent image processing, multidimensional MD image representation and super-resolution 3D image processing and reconstruction, MD computer vision systems, MD multimedia systems, data-based MD image retrieval and knowledge data mining, jamming image recognition and surface defects segmentation, MD signal analysis aimed at medical decision support, MD image processing in robot systems, 3D and multi-view visualization in environmental art, VR and reinforcement learning applications, tensor-based mip map implementation, recursive filtration of MD images and many more. *Digital Phase Lock Loops* Saleh R. Al-Araji, Zahir M. Hussain, Mahmoud A. Al-Qutayri, 2007-04-29 This exciting new book covers various types of digital phase lock loops. It presents a comprehensive coverage of a new class of digital phase lock loops called the time delay tanlock loop (TDTL). It also details a number of architectures that improve the performance of the TDTL through adaptive techniques that overcome the conflicting requirements of the locking range and speed of acquisition. *IEEE Transactions on Circuits and Systems*, 2006. *A Digital FM Demodulator in a Field Programmable Gate Array* Jonathan P. Skroch, 1996. *Digital Signal Processing in Power Electronics Control Circuits* Krzysztof Sozański, 2013-07-03 Many digital control circuits in current literature are described using analog transmittance. This may not always be acceptable, especially if the sampling frequency and power transistor switching frequencies are close to the band of interest. Therefore, a digital circuit is considered as a digital controller rather than an analog circuit. This helps to avoid errors and instability in high frequency components. *Digital Signal Processing in Power Electronics Control Circuits* covers problems concerning the design and realization of digital control algorithms for power electronics circuits using digital signal processing (DSP) methods. This book bridges the gap between power electronics and DSP. The following realizations of digital control circuits are considered: digital signal processors, microprocessors, microcontrollers, programmable digital circuits. Discussed in this book is signal processing starting from analog signal acquisition through its conversion to digital form, methods of its filtration and separation, and ending with pulse control of output power transistors. The book is focused on two applications for the considered methods of digital signal processing: an active power filter and a digital class D power amplifier. The major benefit to readers is the acquisition of specific knowledge concerning discussions on the processing of signals from voltage or current sensors using a digital signal processor and to the signals controlling the output inverter transistors. Included are some Matlab examples for illustration of the considered problems. **Radio Communication Handbook** Mike Dennison, 2007. *Proceedings of ... IEEE International Symposium on Consumer Electronics*, 1997. **Index to IEEE Publications** Institute of Electrical and Electronics Engineers, 1995.

Science Abstracts ,1995 *Electrical & Electronics Abstracts* ,1997 □□□□□□□□ ,2006 *Digital Hilbert*
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1. Understanding the eBook Digital Hilbert Transformers For Fpga Based Phase Locked
 - The Rise of Digital Reading Digital Hilbert Transformers For Fpga Based Phase Locked
 - Advantages of eBooks Over Traditional Books
2. Identifying Digital Hilbert Transformers For Fpga Based Phase Locked
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Digital Hilbert Transformers For Fpga Based Phase Locked

- User-Friendly Interface
- 4. Exploring eBook Recommendations from Digital Hilbert Transformers For Fpga Based Phase Locked
 - Personalized Recommendations
 - Digital Hilbert Transformers For Fpga Based Phase Locked User Reviews and Ratings
 - Digital Hilbert Transformers For Fpga Based Phase Locked and Bestseller Lists
- 5. Accessing Digital Hilbert Transformers For Fpga Based Phase Locked Free and Paid eBooks
 - Digital Hilbert Transformers For Fpga Based Phase Locked Public Domain eBooks
 - Digital Hilbert Transformers For Fpga Based Phase Locked eBook Subscription Services
 - Digital Hilbert Transformers For Fpga Based Phase Locked Budget-Friendly Options
- 6. Navigating Digital Hilbert Transformers For Fpga Based Phase Locked eBook Formats
 - ePub, PDF, MOBI, and More
 - Digital Hilbert Transformers For Fpga Based Phase Locked Compatibility with Devices
 - Digital Hilbert Transformers For Fpga Based Phase Locked Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Digital Hilbert Transformers For Fpga Based Phase Locked
 - Highlighting and Note-Taking Digital Hilbert Transformers For Fpga Based Phase Locked
 - Interactive Elements Digital Hilbert Transformers For Fpga Based Phase Locked
- 8. Staying Engaged with Digital Hilbert Transformers For Fpga Based Phase Locked
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Hilbert Transformers For Fpga Based Phase Locked
- 9. Balancing eBooks and Physical Books Digital Hilbert Transformers For Fpga Based Phase Locked
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Digital Hilbert Transformers For Fpga Based Phase Locked
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Hilbert Transformers For Fpga Based Phase Locked
 - Setting Reading Goals Digital Hilbert Transformers For Fpga Based Phase Locked

- Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Hilbert Transformers For Fpga Based Phase Locked
 - Fact-Checking eBook Content of Digital Hilbert Transformers For Fpga Based Phase Locked
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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