Sardar Vallabhbhai National Institute of Technology Computer Engineering Department B.Tech. II (CO) 3rd Semester Subject: Digital Circuits (EC207) Mid Semester Exam (September-2015)

Time: 1:30 Hr.1

[Total Marks: 30]

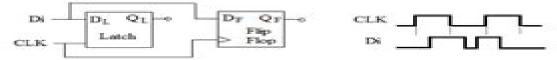
Q.1 (a) Simplify the following expressions:

(5)

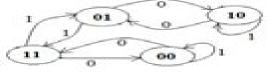
- i) AB'C' + A'B'C'+A'BC'+A'B'C
 ii) ABC+A'BC+AB'C+ABC'+AB'C'+A'BC'+A'B'C'
 iii) A(A+B+C).(A'+B+C).(A+B+C).(A+B+C')
 iv) (A+B+C).(A+B'+C').(A+B+C')
 v) [(AB'+ABC)'+A(B+AB')]'
- (b) Perform BCD Subtraction of the following using 10's complement method:
 i) 983-748
 ii) 786-891
 iii) 649-387

[3]

- Q.2 (a) Plot the logical expression ABCD+AB'C'D'+AB'C+AB on a 4 variable K-MAP; obtain the [2] simplified expression from the map.
 - (b) Using K-Map method, simplify the following function, obtain its Real Minimal Expression [3] along with implementation using universal gate. (Use NAND logic if minimal expression is SOP and NOR logic if minimal expression is POS) f(w, x, y, z) = Σ m (1,3,4,5,6,7,9,12,13)
 - (c) Determine the don't care condition in the following boolean expression BE+B'DE' which is a [2] simplified version of expression A'BE+ BCDE+BC'D'E+A'B'DE'+B'C'DE'
- Q.3 (a) Show all eight entries in characteristics table of JK Flip flop representing Q_(i) as present output [4] and Q_(i+1) as next output. Obtain its next state (i.e. Q_(i+1)) equation.
 - (b) Draw the waveform of output of latch Q_L and output of positive edge triggered flip flop Q_F if [3] Q_L=Q_F=0 initially.



- (c) In SR larch, what will happen if both S and R inputs switch from 1 to 0 simultaneously? Supply [3] your answer with proper diagrams and comments.
- (e) Design and Draw clocked sequential circuit for state diagram shown below using T flip flops. [5]



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and the invaluable mentorship of Avadh Ojha sir will be an indispensable resource for all UPSC aspirants It is our earnest hope that this book will empower candidates to excel in their preparation and achieve their dreams of serving the nation

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