

more detail, in order to understand its fundamental limitations before discussing how to optimize architectures.

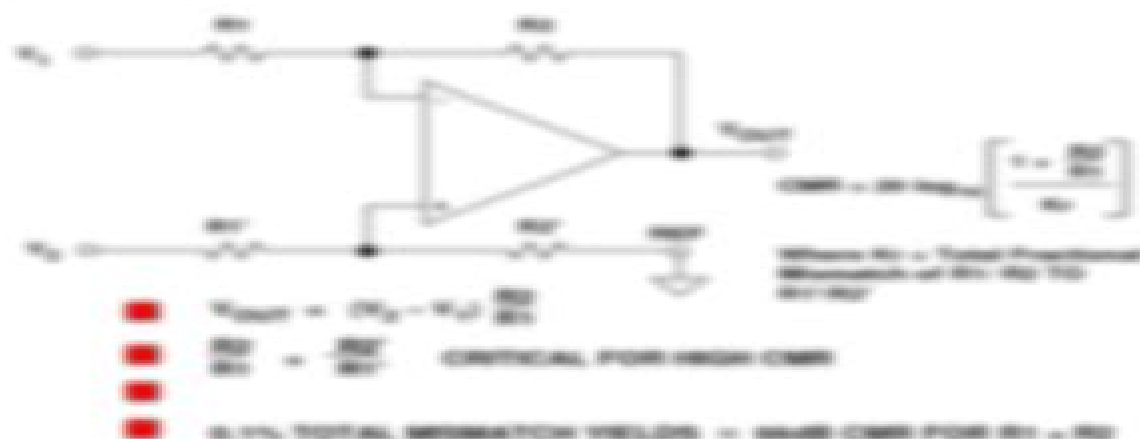


Figure 2: Op Amp Subtractor or Difference Amplifier

There are several fundamental problems with this simple circuit. First, the input impedances seen by V_1 and V_2 isn't balanced. The input impedance seen by V_1 is R_1 , but the input impedance seen by V_2 is $R_2 + R_2$. This configuration can also be quite problematic in terms of CMRR, since even a small resistor impedance imbalance will degrade the available CMRR. This problem can be solved with well-matched open-loop buffers in series with each input (for example, using a precision dual op-amp). But, this adds complexity to a simple circuit, and may introduce offset drift and non-linearity.

The second problem with this circuit is that the CMRR is primarily determined by the resistor ratio matching, not the op-amp. The resistor ratios R_1/R_2 and R_1/R_2 must match extremely well to reject common mode noise—at least as well as a typical op-amp CMRR of >100 dB. Note also that the absolute resistor values are relatively unimportant.

Picking lower 1% resistors from a single batch may yield a net ratio matching of 0.1%, which will achieve a CMRR of 60 dB (assuming $R_1 = R_2$). But if one resistor differs from the rest by 1%, the CMRR will drop to only 40 dB. Clearly, very limited performance is possible using ordinary discrete resistors in this circuit (without resorting to laser matchings). This is because the best standard off-the-shelf 8NC/85NC style resistor tolerances are on the order of 0.1%.

In general, the worst case CMRR for a circuit of this type is given by the following equation:

$$CMRR_{dB} = 20 \log_{10} \left[\frac{1 + R_2/R_1}{\frac{R_2}{R_1}} \right] \quad \text{Eq. 1}$$

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