

100 Power Tips for FPGA Designers

Evgeni Stavinov

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Preface

I've never thought of myself as a book writer. Over the course of my career I've written volumes of technical documentation, published several articles in technical magazines, and have done a lot of technical blogging. At some point I've accumulated a wealth of experience and knowledge in the area of FPGA design, and thought it was a good time to share it with a broader audience.

Writing a book takes time, commitment, and discipline. It also requires a very different skill set. Unfortunately, many engineers, including myself, are trained to use programming languages better than natural languages. Despite all that, writing a book is definitely an intellectually rewarding experience.

I would like to express my gratitude to all the people who have provided valuable ideas, reviewed technical contents, and edited the manuscript: my colleagues from SerialTek, former colleagues from Xilinx, technical bloggers, and many others.

About the Author

Evgeni Stavinov is a longtime FPGA user with more than 10 years of diverse design experience. Before becoming a hardware architect at SerialTek LLC, he held different engineering positions at Xilinx, LeCroy and CATC. Evgeni holds MS and BS degrees in electrical engineering from University of Southern California and Technion - Israel Institute of Technology. Evgeni is a creator of OutputLogic.com, a portal that offers different online productivity tools.

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100 Power Tips for FPGA Designers , **Design Recipes for FPGAs** Peter Wilson,2015-10-01 Design Recipes for FPGAs provides a rich toolbox of design techniques and templates to solve practical every day problems using FPGAs Using a modular structure it provides design techniques and templates at all levels together with functional code which you can easily match and apply to your application Written in an informal and easy to grasp style this invaluable resource goes beyond the principles of FPGAs and hardware description languages to demonstrate how specific designs can be synthesized simulated and downloaded onto an FPGA In addition the book provides advanced techniques to create real world designs that fit the device required and which are fast and reliable to implement Examples are rewritten and tested in Verilog and VHDL Describes high level applications as examples and provides the building blocks to implement them enabling the student to start practical work straight away Singles out the most important parts of the language that are needed for design giving the student the information needed to get up and running quickly **Advanced FPGA Design** Steve Kilts,2007-07-13 This book provides the advanced issues of FPGA design as the underlying theme of the work In practice an engineer typically needs to be mentored for several years before these principles are appropriately utilized The topics that will be discussed in this book are essential to designing FPGA s beyond moderate complexity The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real world experience **FPGA Design Automation** Deming Chen,Jason Cong,Peichen Pan,2006 FPGA Design Automation A Survey is an up to date comprehensive survey tutorial of FPGA design automation with an emphasis on the recent developments within the past 5 to 10 years The focus is on the theory and techniques that have been or most likely will be reduced to practice It covers all major steps in FPGA design flow routing and placement circuit clustering technology mapping and architecture specific optimization physical synthesis RT level and behavior level synthesis and power optimization FPGA Design Automation A Survey can be used as both a guide for beginners who are embarking on research in this relatively young yet exciting area and a useful reference for established researchers in this field **FPGA Design** Philip Simpson,2010-07-23 In August of 2006 an engineering VP from one of Altera s customers approached Misha Burich VP of Engineering at Altera asking for help in reliably being able to predict the cost schedule and quality of system designs reliant on FPGA designs At this time I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process I noted that this problem was not unique to this one customer The characteristics of the problem are shared by many Corporations that implement designs in FPGAs The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams There is a wide range of design experience across the teams There is no working process for sharing design blocks between engineering teams As I analyzed the data that I had received from hundreds of customer visits in the

past I noticed that design reuse among engineering teams was a challenge I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies Altera had recently solved this problem as part of its own FPGA design software and IP development process

FPGA-Based System Design Wayne Hendrix Wolf, 2004 Everything FPGA designers need to know about FPGAs and VLSI Digital designs once built in custom silicon are increasingly implemented in field programmable gate arrays FPGAs Effective FPGA system design requires a strong understanding of VLSI issues and constraints and an understanding of the latest FPGA specific techniques In this book Princeton University's Wayne Wolf covers everything FPGA designers need to know about all these topics both the how and the why Wolf begins by introducing the essentials of VLSI fabrication circuits interconnects combinational and sequential logic design system architectures and more Next he demonstrates how to reflect this VLSI knowledge in a state of the art design methodology that leverages FPGA's most valuable characteristics while mitigating its limitations Coverage includes How VLSI characteristics affect FPGAs and FPGA based logic design How classical logic design techniques relate to FPGA based logic design Understanding FPGA fabrics the basic programmable structures of FPGAs Specifying and optimizing logic to address size speed and power consumption Verilog VHDL and software tools for optimizing logic and designs The structure of large digital systems including register transfer design methodology Building large scale platform and multi FPGA systems A start to finish DSP case study addressing a wide range of design problems PRENTICE HALL Professional Technical Reference Upper Saddle River NJ 07458 www.phptr.com ISBN 0 13 142461 0

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis Sumit Ahuja, Avinash Lakshminarayana, Sandeep Kumar Shukla, 2011-10-21 This book presents novel research techniques algorithms methodologies and experimental results for high level power estimation and power aware high level synthesis Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC FPGA design

The Design Warrior's Guide to FPGAs Clive Maxfield, 2004-04-26 Field Programmable Gate Arrays FPGAs are devices that provide a fast low cost way for embedded system designers to customize products and deliver new versions with upgraded features because they can handle very complicated functions and be reconfigured an infinite number of times In addition to introducing the various architectural features available in the latest generation of FPGAs The Design Warrior's Guide to FPGAs also covers different design tools and flows This book covers information ranging from schematic driven entry through traditional HDL RTL based simulation and logic synthesis all the way up to the current state of the art in pure C/C++ design capture and synthesis technology Also discussed are specialist areas such as mixed hardware software and DSP based design flows along with innovative new devices such as field programmable node arrays FPNAs Clive Maxfield is a bestselling author and engineer with a large following in the electronic design automation EDA and embedded systems industry In this comprehensive book he covers all the issues of interest to designers working with or

contemplating a move to FPGAs in their product designs While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems First book to focus exclusively and comprehensively on FPGA use in embedded designs World renowned best selling author Will help engineers get familiar and succeed with this new technology by providing much needed advice on choosing the right FPGA for any design project

FPGA Design Philip Andrew Simpson, 2015-05-19 This book describes best practices for successful FPGA design It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams By gaining an understanding into their design environments processes what works and what does not work key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed This book's content has a strong focus on design teams that are spread across sites The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams enabling the exchange of design blocks across teams Coverage includes the complete FPGA design flow from the basics to advanced techniques This new edition has been enhanced to include new sections on System modeling embedded design and high level design The original sections on Design Environment RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers Presents complete field tested methodology for FPGA design focused on reuse across design teams Offers best practices for FPGA timing closure in system debug and board design Details techniques to resolve common pitfalls in designing with FPGAs

Design Recipes for FPGAs Peter Robert Wilson, 2007 This book is an essential desktop reference containing a rich toolbox of design techniques and templates for solving practical every day problems using FPGAs Written in an informal and easy to grasp style this invaluable resource shows how specific designs can be synthesized and downloaded onto an FPGA In addition the book provides advanced techniques to create real world designs which are fast and reliable to implement

FPGA-Based System Design Wolf, 1900 This is the eBook version of the printed book If the print book includes a CD ROM this content is not included within the eBook version Everything FPGA designers need to know about FPGAs and VLSI Digital designs once built in custom silicon are increasingly implemented in field programmable gate arrays FPGAs Effective FPGA system design requires a strong understanding of VLSI issues and constraints and an understanding of the latest FPGA specific techniques In this book Princeton University's Wayne Wolf covers everything FPGA designers need to know about all these topics both the

FPGAs and Programmable LSI Geoff Bostock, 1996 This is the most comprehensive practical guide to designing with FPGAs and programmable LSI Programmable logic devices PLDs have been in general use for over twenty years The demands of modern electronic design mean that traditional PAL technology has given way to a powerful new approach field programmable gate array FPGA technology This book shows a designer how to choose the appropriate FPGA and design method for any application It also gives hints and tips based on the author's wide experience in the field to

allow designers to optimise performance of any particular family of devices The design process for an FPGA needs to be far more rigorous than for PAL since troubleshooting is far harder to perform There are moreover a dozen or more manufacturers of FPGAs each with a different architecture and performance so choosing the right device for any particular application is a critical part of the design process Similarly there are various design methods each with particular features This book covers them all and gives a designer the benefit of Geoff Bostock s valuable experience First design guide published on FPGAs Full of data never previously compiled Based on real design experience of making FPGAs and programmable LSI work Power Optimization and Prediction Techniques for FPGAs [microform] Jason Helge Anderson,2005 Following this the circuit level design of low power FPGA interconnect is considered A family of new low power FPGA routing switches is proposed The switches significantly reduce dynamic and leakage power in the interconnect with varying amounts of area and or performance cost The proposed switches require only minor changes to traditional FPGA routing switches allowing them to be easily incorporated into current FPGAs Field programmable gate arrays FPGAs are a popular choice for digital circuit implementation because of their growing density and speed short design cycle and steadily decreasing cost Power consumption specifically leakage power has become a major concern for the semi conductor industry and its customers FPGAs are less power efficient than custom ASICs due to the overhead required to provide programmability Despite this power has been largely ignored by the FPGA research community whose prime focus to date has centered on improving FPGA speed and area efficiency This dissertation presents new techniques for optimizing and predicting the power consumption of FPGAs First two novel computer aided design CAD techniques for FPGA leakage power reduction are presented The proposed techniques are unique in that they substantially reduce leakage power while imposing no cost meaning that they have no impact on FPGA area efficiency speed or fabrication cost Finally the topic of early dynamic power estimation for FPGAs is addressed Empirical models are developed for the prediction of interconnect capacitance and switching activity in FPGA designs The proposed models can be applied early in the design process when detailed routing data is incomplete or unavailable thereby reducing design effort and cost Next a new power aware technology mapping algorithm for look up table based FPGAs is described The algorithm takes an activity conscious approach to logic replication and allows trade offs between circuit performance and power The dynamic power of mapping solutions produced by the proposed algorithm is shown to be considerably less than competing techniques *FPGA Design* Philip Andrew Simpson,2010-08-11 In August of 2006 an engineering VP from one of Altera s customers approached Misha Burich VP of Engineering at Altera asking for help in reliably being able to predict the cost schedule and quality of system designs reliant on FPGA designs At this time I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process I noted that this problem was not unique to this one customer The characteristics of the

problem are shared by many Corporations that implement designs in FPGAs The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams There is a wide range of design experience across the teams There is no working process for sharing design blocks between engineering teams As I analyzed the data that I had received from hundreds of customer visits in the past I noticed that design reuse among engineering teams was a challenge I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies Altera had recently solved this problem as part of its own FPGA design software and IP development process **Learning FPGAs** Justin Rajewski,2017

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