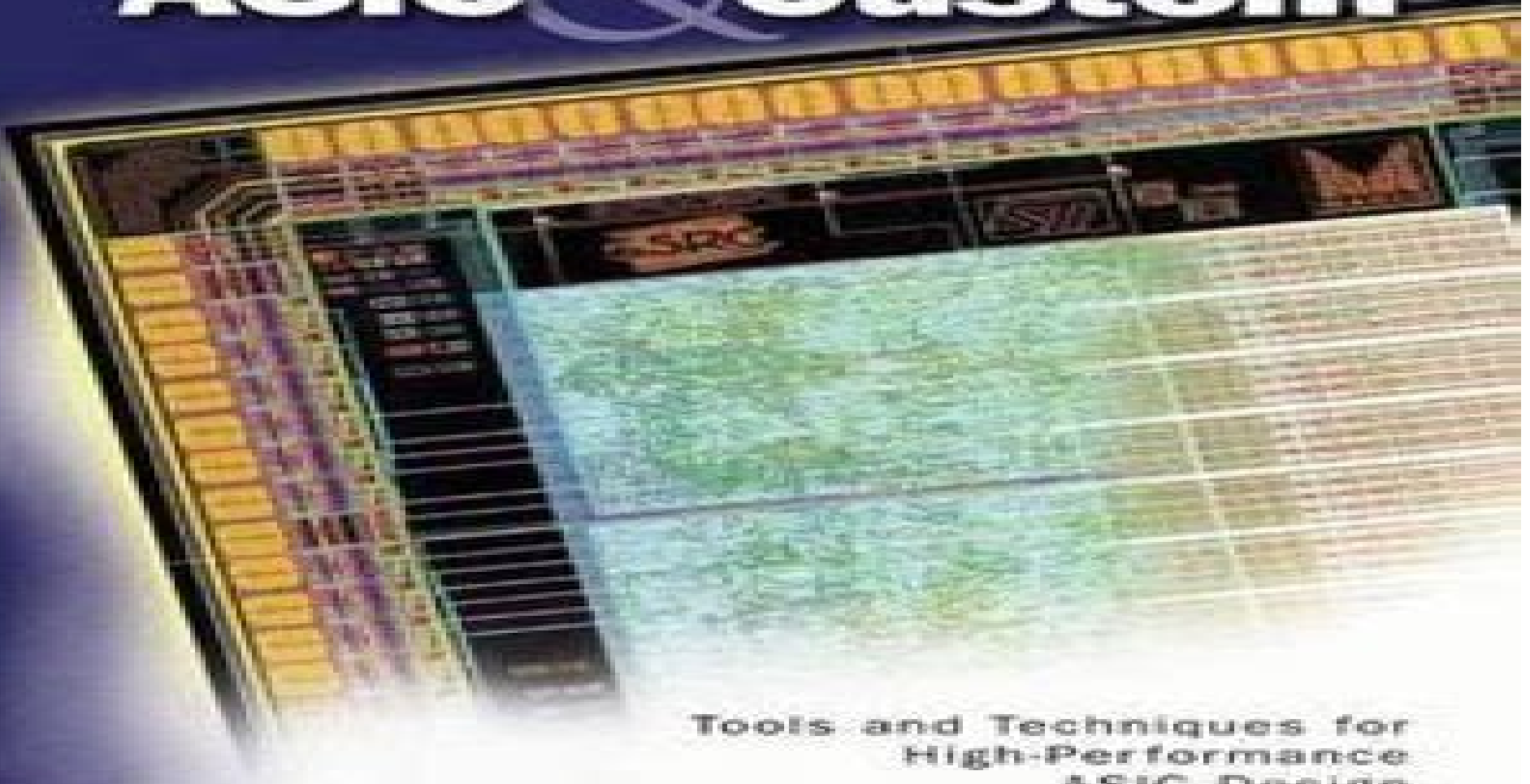


CLOSING THE GAP BETWEEN **ASIC & Custom**



Tools and Techniques for
High-Performance
ASIC Design

**David Chinnery
Kurt Keutzer**

**Closing The Gap Between Asic And Custom Tools And
Techniques For High Performance Asic Design Author
David Chinnery Jun**

Khosrow Golshan



Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun :

Closing the Gap Between ASIC & Custom David Chinnery, Kurt Keutzer, 2007-05-08 by Kurt Keutzer Those looking for a quick overview of the book should fast forward to the Introduction in Chapter 1 What follows is a personal account of the creation of this book The challenge from Earl Killian formerly an architect of the MIPS processors and at that time Chief Architect at Tensilica was to explain the significant performance gap between ASICs and custom circuits designed in the same process generation The relevance of the challenge was amplified shortly thereafter by Andy Bechtolsheim founder of Sun Microsystems and ubiquitous investor in the EDA industry At a dinner talk at the 1999 International Symposium on Physical Design Andy stated that the greatest near term opportunity in CAD was to develop tools to bring the performance of ASIC circuits closer to that of custom designs There seemed to be some synchronicity that two individuals so different in concern and character would be pre occupied with the same problem Intrigued by Earl and Andy s comments the game was afoot Earl Killian and other veterans of microprocessor design were helpful with clues as to the sources of the performance discrepancy layout circuit design clocking methodology and dynamic logic I soon realized that I needed help in tracking down clues Only at a wonderful institution like the University of California at Berkeley could I so easily commandeer an ab bodied graduate student like David Chinnery with a knowledge of architecture circuits computer aided design and algorithms

Closing the Power Gap between ASIC & Custom David Chinnery, Kurt Keutzer, 2008-01-23 Explains how to use low power design in an automated design flow and examine the design time and performance trade offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology a much neglected area

Forthcoming Books Rose Arny, 2002 Successful ASIC Design the First Time Through John Huber, 2012-11-16 he very name application specific integrated circuit or ASIC con T notes an ability to provide a dense package for a highly complex design targeted at a focused often complex solution The ability to create customized high performance designs has come of age facilitated by so phisticated tools that enable designers to cope with ever increasing demands for added product functionality features and complexity Most designers are trained in the traditional methods of approaching complex digital electronics with standard parts but have little if any exposure to custom or even semicustom integrated circuit design Most see only a broad survey of IC technology This book is targeted at the new ASIC designer who is getting ready to tackle that first ASIC design and is concerned about the unknowns that lie ahead Economic and performance considerations as well as tool capability and process fabrication quality have evolved to the point where consideration of ASIC design is now commonplace in an ever increasing number of electronic systems designs Engineers are now given the challenge of coping not only with new technologies but with new design methodologies that are fundamen tally necessary and advantageous to support new competitive high tech products Laypeople and engineers alike have marveled at the

advances made over the years in electronics complexity performance density and cost The migration of systems to modules to boards to integrated circuits clearly underscores the radical transition that the physical incarnation of electronics has undergone

Successful ASIC Design the First Time Through John Huber,2013-05-14 he very name application specific integrated circuit or ASIC con T notes an ability to provide a dense package for a highly complex design targeted at a focused often complex solution The ability to create customized high performance designs has come of age facilitated by so phisticated tools that enable designers to cope with ever increasing de mands for added product functionality features and complexity Most designers are trained in the traditional methods of approaching complex digital electronics with standard parts but have little if any exposure to custom or even semicustom integrated circuit design Most see only a broad survey of IC technology This book is targeted at the new ASIC designer who is getting ready to tackle that first ASIC design and is concerned about the unknowns that lie ahead Economic and perfor mance considerations as well as tool capability and process fabrication quality have evolved to the point where consideration of ASIC design is now commonplace in an ever increasing number of electronic systems designs Engineers are now given the challenge of coping not only with new technologies but with new design methodologies that are fundamen tally necessary and advantageous to support new competitive high tech products Laypeople and engineers alike have marveled at the advances made over the years in electronics complexity performance density and cost The migration of systems to modules to boards to integrated circuits clearly underscores the radical transition that the physical incarnation of electronics has undergone

From ASICs to SOCs Farzad Nekoogar,Faranak Nekoogar,2003 From ASICs to SOCs A Practical Approach by Farzad Nekoogar and Faranak Nekoogar covers the techniques principles and everyday realities of designing ASICs and SOCs Material includes current issues in the field front end and back end designs integration of IPs on SOC designs and low power design techniques and methodologies Appropriate for practicing chip designers as well as graduate students in electrical engineering

The Art of Timing Closure Khosrow Golshan,2020-08-03 The Art of Timing Closure is written using a hands on approach to describe advanced concepts and techniques using Multi Mode Multi Corner MMMC for an advanced ASIC design implementation It focuses on the physical design Static Timing Analysis STA formal and physical verification The scripts in this book are based on Cadence Encounter System™ However if the reader uses a different EDA tool that tool s commands are similar to those shown in this book The topics covered are as follows Data Structures Multi Mode Multi Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth the author emphasizes short clear descriptions which are implemented by references to authoritative manuscripts It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise This book is intended for anyone who is involved in ASIC design implementation starting from physical

design to final design signoff Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design *High Performance ASIC Design* Razak Hossain, 2008-08-21 A methodology for using domino logic in an ASIC design flow for graduate students researchers and circuit designers in industry

Signal Integrity Effects in Custom IC and ASIC Designs Raminderpal Singh, 2001-12-12 offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity Jake Buurma Senior Vice President Worldwide Research Development Cadence Design Systems Inc Covers signal integrity effects in high performance Radio Frequency RF IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future A Wiley IEEE Press publication Surviving the ASIC Experience John Schroeter, 1992 The strategies in this handbook will tremendously increase the Application Specific Integrated Circuits ASIC user's chances of success Proven procedures help the user achieve a chip working on first pass at speed in the system on time within budget and without pain Real world issues as they relate to ASIC are dealt with from a viewpoint of implementation and project management The guide will benefit electronics engineering and management personnel employed in aerospace and defense industrial telecom electronic data processing automotive and consumer electronics industries KEY FEATURES guidelines on select the appropriate ASIC technologies and methodologies comes with test program development procedures shows the user how to beat the high failure rate in ASIC and VLSI technology techniques to help remove the burden of the long schedules high costs and high risk factor associated with ASIC John Schroeter has held ASIC engineering project management and marketing management posts with CADIC Fairchild Semiconductor and Seattle Silicon

Quick-Turnaround ASIC Design in VHDL N. Bouden-Romdhane, Vijay Madiseti, J.W. Hines, 2012-12-06 From the Foreword Modern digital signal processing applications provide a large challenge to the system designer Algorithms are becoming increasingly complex and yet they must be realized with tight performance constraints Nevertheless these DSP algorithms are often built from many constituent canonical subtasks e.g. IIR and FIR filters FFTs that can be reused in other subtasks Design is then a problem of composing these core entities into a cohesive whole to provide both the intended functionality and the required performance In order to organize the design process there have been two major approaches The top down approach starts with an abstract concise functional description which can be quickly generated On the other hand the bottom up approach starts from a detailed low level design where performance can be directly assessed but where the requisite design and interface detail take a long time to generate In this book the authors show a way to effectively resolve this tension by retaining the high level conciseness of VHDL while parameterizing it to get good fit to specific applications through reuse of core library components Since they build on a pre designed set of core elements accurate area speed and power estimates can be percolated to high level design routines which explore the design space Results are impressive and the cost model provided will prove to be very useful Overall the authors have provided an

up to date approach doing a good job at getting performance out of high level design The methodology provided makes good use of extant design tools and is realistic in terms of the industrial design process The approach is interesting in its own right but is also of direct utility and it will give the existing DSP CAD tools a highly competitive alternative The techniques described have been developed within ARPAs RASSP Rapid Prototyping of Application Specific SignalProcessors project and should be of great interest there as well as to many industrial designers Professor Jonathan Allen Massachusetts Institute of Technology

High Level Synthesis of ASICs under Timing and Synchronization Constraints David C. Ku,Giovanni DeMicheli,2013-03-14 Computer aided synthesis of digital circuits from behavioral level specifications offers an effective means to deal with increasing complexity of digital hardware design High Level Synthesis of ASICs Under Timing and Synchronization Constraints addresses both theoretical and practical aspects in the design of a high level synthesis system that transforms a behavioral level description of hardware to a synchronous logic level implementation consisting of logic gates and registers High Level Synthesis of ASICs Under Timing and Synchronization Constraints addresses specific issues in applying high level synthesis techniques to the design of ASICs This complements previous results achieved in synthesis of general purpose and signal processors where data path design is of utmost importance In contrast ASIC designs are often characterized by complex control schemes to support communication and synchronization with the environment The combined design of efficient data path control unit is the major contribution of this book Three requirements are important in modeling ASIC designs concurrency external synchronization and detailed timing constraints The objective of the research work presented here is to develop a hardware model incorporating these requirements as well as synthesis algorithms that operate on this hardware model The contributions of this book address both the theory and the implementation of algorithm for hardware synthesis

ASIC Design and Synthesis Vaibbhav Taraate,2021-01-06 This book describes simple to complex ASIC design practical scenarios using Verilog It builds a story from the basic fundamentals of ASIC designs to advanced RTL design concepts using Verilog Looking at current trends of miniaturization the contents provide practical information on the issues in ASIC design and synthesis using Synopsys DC and their solution The book explains how to write efficient RTL using Verilog and how to improve design performance It also covers architecture design strategies multiple clock domain designs low power design techniques DFT pre layout STA and the overall ASIC design flow with case studies The contents of this book will be useful to practicing hardware engineers students and hobbyists looking to learn about ASIC design and synthesis

Advanced ASIC Chip Synthesis Himanshu Bhatnagar,2002 This book describes advanced concepts and techniques for ASIC chip synthesis physical synthesis formal verification and static timing analysis using the Synopsys suite of tools The ASIC design flow methodology targeted for very deep sub micron VDSM technologies is also covered in detail Emphasis is on real time application of Synopsys tools used to combat various problems seen at VDSM geometries A design methodology is presented for handling complex sub micron ASIC designs At each step problems related to each phase of the

design flow are identified and solutions are described The target audiences for this book are practicing ASIC design engineers and masters level students in advanced VLSI courses on ASIC chip design and DFT techniques This second edition is updated to the Tcl version of Design Compiler Bhatnagar is an ASIC Design Group Leader in a semiconductor company Annotation copyrighted by Book News Inc Portland OR **An ASIC Low Power Primer** Rakesh Chadha,J. Bhasker,2012-12-05 This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices Readers will benefit from the hands on approach which starts from the ground up explaining with basic examples what power is how it is measured and how it impacts on the design process of application specific integrated circuits ASICs The authors use both the Unified Power Format UPF and Common Power Format CPF to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent From analyzing system power consumption to techniques that can be employed in a low power design to a detailed description of two alternate standards for capturing the power directives at various phases of the design this book is filled with information that will give ASIC designers a competitive edge in low power design **Advanced ASIC Chip Synthesis** Himanshu Bhatnagar,2012-11-11 Advanced ASIC Chip Synthesis Using Synopsys Design Compiler and PrimeTime describes the advanced concepts and techniques used for ASIC chip synthesis formal verification and static timing analysis using the Synopsys suite of tools In addition the entire ASIC design flow methodology targeted for VDSM Very Deep Sub Micron technologies is covered in detail The emphasis of this book is on real time application of Synopsys tools used to combat various problems seen at VDSM geometries Readers will be exposed to an effective design methodology for handling complex sub micron ASIC designs Significance is placed on HDL coding styles synthesis and optimization dynamic simulation formal verification DFT scan insertion links to layout and static timing analysis At each step problems related to each phase of the design flow are identified with solutions and work arounds described in detail In addition crucial issues related to layout which includes clock tree synthesis and back end integration links to layout are also discussed at length Furthermore the book contains in depth discussions on the basics of Synopsys technology libraries and HDL coding styles targeted towards optimal synthesis solutions Advanced ASIC Chip Synthesis Using Synopsys Design Compiler and PrimeTime is intended for anyone who is involved in the ASIC design methodology starting from RTL synthesis to final tape out Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques From the Foreword This book written by Himanshu Bhatnagar provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsys suite of tools It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration offront end and back end tools Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows The author provides numerous practical examples derived from real world situations

that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design

Dr Dwight W Decker Chairman and CEO Conexant Systems Inc Formerly Rockwell Semiconductor Systems Newport Beach CA USA

Physical Design Essentials Khosrow Golshan, 2007-04-08 Arranged in a format that follows the industry common ASIC physical design flow Physical Design Essentials begins with general concepts of an ASIC library then examines floorplanning placement routing verification and finally testing Among the topics covered are Basic standard cell design transistor sizing and layout styles Linear non linear and polynomial characterization Physical design constraints and floorplanning styles Algorithms used for placement Clock Tree Synthesis Parasitic extraction Electronic Testing and many more

Application-specific Integrated Circuits Michael John Sebastian Smith, 1997 This comprehensive book on application specific integrated circuits ASICs describes the latest methods in VLSI systems design ASIC design using commercial tools and pre designed cell libraries is the fastest most cost effective and least error prone method of IC design As a consequence ASICs and ASIC design methods have become increasingly popular in industry for a wide range of applications The book covers both semicustom and programmable ASIC types After describing the fundamentals of digital logic design and the physical features of each ASIC type the book turns to ASIC logic design design entry logic synthesis simulation and test and then to physical design partitioning floorplanning placement and routing You will find here in practical well explained detail everything you need to know to understand the design of an ASIC and everything you must do to begin and to complete your own design Features Broad coverage includes in one information packed volume cell based ICs gate arrays field programmable gate arrays FPGAs and complex programmable logic devices PLDs Examples throughout the book have been checked with a wide range of commercial tools to ensure their accuracy and utility Separate chapters and appendixes on both Verilog and VHDL including material from IEEE standards serve as a complete reference for high level ASIC design entry As in other landmark VLSI books published by Addison Wesley from Mead and Conway to Weste and Eshraghian the author's teaching expertise and industry experience illuminate the presentation of useful design methods Any engineer manager or student who is working with ASICs in a design project or who is simply interested in knowing more about the different ASIC types and design styles will find this book to be an invaluable resource reference and guide

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Designing with High Performance ASICs Joseph Di Giacomo, 1992 Discussing ASIC techniques of designing troubleshooting and evaluating application specific integrated circuit chips this book explores the concepts principles and methods of high performance ASIC design It covers the pros and cons of CAD tools and discusses product customization

Application Specific Integrated Circuit (ASIC) Technology Norman Einspruch, 2012-12-02 Application Specific Integrated Circuit ASIC Technology explores and discusses the different aspects of the ASIC technology experienced during the 1990s The topics of the chapters range from the ASIC business model marketing and development up to its testability packaging and quality and reliability An introductory chapter begins the discussion and tackles the historical

perspective and the classification of the ASIC technology Chapters 2 and 3 cover the business side of the technology as it discusses the market dynamics and marketing strategies The following chapters focus on the product itself and deal with the design and model and library development Computer aided design tools and systems are included in the discussion Manufacturing and packaging of ASICs are also given attention in the book Finally the last three chapters present the application testability and reliability of ASIC technology The text can be of most help to students in the fields of microelectronics computer technology and engineering

The book delves into Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun . Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun is a crucial topic that needs to be grasped by everyone, from students and scholars to the general public. The book will furnish comprehensive and in-depth insights into Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun , encompassing both the fundamentals and more intricate discussions.

1. The book is structured into several chapters, namely:
 - Chapter 1: Introduction to Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun
 - Chapter 2: Essential Elements of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun
 - Chapter 3: Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun in Everyday Life
 - Chapter 4: Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun in Specific Contexts
 - Chapter 5: Conclusion
2. In chapter 1, this book will provide an overview of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun . This chapter will explore what Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun is, why Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun is vital, and how to effectively learn about Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun .
3. In chapter 2, the author will delve into the foundational concepts of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun . The second chapter will elucidate the essential principles that must be understood to grasp Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun in its entirety.
4. In chapter 3, this book will examine the practical applications of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun in daily life. The third chapter will showcase real-world examples of how Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design

Author David Chinnery Jun can be effectively utilized in everyday scenarios.

5. In chapter 4, the author will scrutinize the relevance of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun in specific contexts. The fourth chapter will explore how Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun is applied in specialized fields, such as education, business, and technology.
6. In chapter 5, this book will draw a conclusion about Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun . This chapter will summarize the key points that have been discussed throughout the book.

The book is crafted in an easy-to-understand language and is complemented by engaging illustrations. This book is highly recommended for anyone seeking to gain a comprehensive understanding of Closing The Gap Between Asic And Custom Tools And Techniques For High Performance Asic Design Author David Chinnery Jun .

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