Automatic Placement and Routing using Cadence Encounter

6.375 Totorial 5 February 12, 2007

In this tutorial you will gain experience using Cadence Encounter to perform automatic placement and routing. A place+route tool takes a gate-level netlist as input and first determines how each gate should be placed on the chip. It uses several heuristic algorithms to group related gates together and thus hopefully minimize routing congestion and wire delay. Place+route tools will focus their effort on minimizing the delay through the critical path. To this end, these tools can resize gates, insert new buffers, and even perform local resynthesis. Place+route tools often have additional algorithms to help reduce area for non-critical paths. After placement, the place+route tool will attempt to route the design while minimizing wire delay. Place+route tools often include additional facilities for clock tree synthesis, power routing, and block level floorplanning. Figure 1 shows how Encounter fits into the 6-375 toolibor.

The following documentation is located in the course locker (/mit/6.375/doc) and provides additional information about Encounter and the Tower 0.18 µm Standard Cell Library.

- tel-180m-sc-databook.pdf Dutubook for Tower 0.18 jum Standard Cell Library
- encounter-user-guide.pdf Encounter user guide
- encounter-command-line-ref.pdf Encounter text command reference
- encounter-menu-ref.pdf Encounter GUI reference

Getting started

Before using the 6,375 toolflow you must add the course locker and run the course setup script with the following two communies.

% add 6.375 % adurce /wit/6.375/setup.csh

For this tutorial we will be using an unpipelimed SMIPSv1 processor as our example RTL design. You should create a working directory and checkent the SMIPSv1 example project from the course CVS repository using the following communicis.

% mkdir tut5 % cd tut5 % cvs checkout examples/smipsvi-istage-w % cd examples/smipsvi-istage-v

Before starting, take a look at the sub-directories in the smigpt1-intage-v project directory. Figure 2 shows the system diagram which is implemented by the example code. When pushing designs through the physical toulflow we will often refer to the case. The core module contains everything which will be on-chip, while blocks outside the core are assume to be off-thip. For this tutorial we are assuming that the processor and a combinational memory are located within the core. A combinational memory means that the read address is specified at the beginning of the cycle, and

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VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design Andreas Burg, Ayse Coskun, Matthew Guthaus, Srinivas Katkoori, Ricardo Reis, 2013-11-26 This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10 5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2012 held in Santa Cruz CA USA in October 2012 The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system design levels as well as in the test of these systems **Energy-Efficient Communication** Processors Robert Fasthuber, Francky Catthoor, Prayeen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author's design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater Euro-Par 2007 Workshops: Parallel Processing Luc Bougé, 2008-02-29 This scalability to future process technology nodes book constitutes the thoroughly refereed joint post workshop proceedings of three international events the International Workshop on Highly Parallel Processing on a Chip HPPC 2007 the UNICORE Summit 2007 and the Workshop on Virtualization Xen in High Performance Cluster and Grid Computing VHPC 2007 held in Rennes France in August 2007 within the scope of Euro Par 2007 the 13th International Conference on Parallel Computing The 8 papers of the HHPC 2007 workshop address all aspects of existing and emerging envisaged multi core processors with a significant amount of parallelism especially to considerations on novel paradigms and models and the related architectural and linguistic support The 8 papers presented at the UNICORE Summit 2007 show current developments and implementations of the UNICORE middleware system a grid technology providing a seamless secure and intuitive access to distributed Grid resources UNICORE is a full grown and well tested Grid middleware system which today is used in daily production worldwide The 9 papers of the VHPC 2007 workshop present new models for implementing high performance computing HPC architectures in both cluster and grid environments and cover areas including performance of virtual machine monitors VMM VMM architecture and implementation cluster and grid VMM applications management of VM based computing resources and hardware support for virtualization Transactions on Computational Science IV Marina Gavrilova, C. J. Kenneth Tan, 2009-04-22 The LNCS journal Transactions on Computational Science reflects recent developments in the field of Computational Science conceiving the field not as a mere ancillary science but rather as an innovative approach supporting

many other scientific disciplines The journal focuses on original high quality research in the realm of computational science in parallel and distributed environments encompassing the facilitating theoretical foundations and the applications of large scale computations and massive data processing It addresses researchers and practitioners in areas ranging from aerospace to biochemistry from electronics to geosciences from mathematics to software architecture presenting verifiable computational methods findings and solutions and enabling industrial users to apply techniques of leading edge large scale high performance computational methods This issue focuses on the theme of security in computing a topic of vital importance in the increasingly connected world of today The 14 extensive papers selected for inclusion in this volume give an in depth coverage of a number of hot topics in the field presenting new architectures novel hardware implementations cryptographic algorithms and security protocols and new tools and applications **Design Automation and Applications for Emerging Reconfigurable Nanotechnologies** Shubham Rai, Akash Kumar, 2023-09-11 This book is a single source solution for anyone who is interested in exploring emerging reconfigurable nanotechnology at the circuit level It lays down a solid foundation for circuits based on this technology having considered both manual as well as automated design flows The authors discuss the entire design flow consisting of both logic and physical synthesis for reconfigurable nanotechnology based circuits The authors describe how transistor reconfigurable properties can be exploited at the logic level to have a more efficient circuit design flow as compared to conventional design flows suited for CMOS Further the book provides insights into hardware security features that can be intrinsically developed using the runtime reconfigurable features of this nanotechnology

Tree-based Heterogeneous FPGA Architectures Umer Faroog, Zied Marrakchi, Habib Mehrez, 2012-05-17 This book presents a new FPGA architecture known as tree based FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures High Performance and Energy Efficient Multi-core Systems for DSP Applications Zhiyi Yu,2007 **Data Acquisition** Michele Vadursi, 2010-11-28 The book is intended to be a collection of contributions providing a bird's eye view of some relevant multidisciplinary applications of data acquisition While assuming that the reader is familiar with the basics of sampling theory and analog to digital conversion the attention is focused on applied research and industrial applications of data acquisition Even in the few cases when theoretical issues are investigated the goal is making the theory comprehensible to a wide application oriented audience **Designing Reliable** and Efficient Networks on Chips Srinivasan Murali, 2009-05-26 Developing NoC based interconnect tailored to a particular application domain satisfying the application performance constraints with minimum power area overhead is a major challenge With technology scaling as the geometries of on chip devices reach the physical limits of operation another important design challenge for NoCs will be to provide dynamic run time support against permanent and intermittent faults

that can occur in the system The purpose of Designing Reliable and Efficient Networks on Chips is to provide state of the art methods to solve some of the most important and time intensive problems encountered during NoC design FPGA ... ,2006

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analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck EDN, 2005

Publications Combined - Over 100 Studies In Proceedings ,2003 EDN, Electrical Design News ,2002 Nanotechnology With Medical, Military And Industrial Applications 2008-2017, Over 7 300 total pages Just a sample of the contents Title Multifunctional Nanotechnology Research Descriptive Note Technical Report 01 Jan 2015 31 Jan 2016 Title Preparation of Solvent Dispersible Graphene and its Application to Nanocomposites Descriptive Note Technical Report Title Improvements To Micro Contact Performance And Reliability Descriptive Note Technical Report Title Delivery of Nanotethered Therapies to Brain Metastases of Primary Breast Cancer Using a Cellular Trojan Horse Descriptive Note Technical Report 15 Sep 2013 14 Sep 2016 Title Nanotechnology Based Detection of Novel microRNAs for Early Diagnosis of Prostate Cancer Descriptive Note Technical Report 15 Jul 2016 14 Jul 2017 Title A Federal Vision for Future Computing A Nanotechnology Inspired Grand Challenge Descriptive Note Technical Report Title Quantifying Nanoparticle Release from Nanotechnology Scientific Operating Procedure Series SOP C 3 Descriptive Note Technical Report Title Synthesis Characterization And Modeling Of Functionally Graded Multifunctional Hybrid Composites For Extreme Environments Descriptive Note Technical Report 15 Sep 2009 14 Mar 2015 Title Equilibrium Structures and Absorption Spectra for SixOy Molecular Clusters using Density Functional Theory Descriptive Note Technical Report Title Nanotechnology for the Solid Waste Reduction of Military Food Packaging Descriptive Note Technical Report 01 Apr 2008 01 Jan 2015 Title Magneto Electric Conversion of Optical Energy to Electricity Descriptive Note Final performance rept 1 Apr 2012 31 Mar 2015 Title Surface Area Analysis Using the Brunauer Emmett Teller BET Method Standard Operating Procedure Series SOP C Descriptive Note Technical Report 30 Sep 2015 30 Sep 2016 Title Stabilizing Protein Effects on the Pressure Sensitivity of Fluorescent Gold Nanoclusters Descriptive Note Technical Report Title Theory Guided Innovation of Noncarbon Two Dimensional Nanomaterials Descriptive Note Technical Report 14 Feb 2012 14 Feb 2016 Title Deterring Emergent Technologies Descriptive Note Journal Article Title The Human Domain and the Future of Army Warfare Present as Prelude to 2050 Descriptive Note Technical Report Title Drone Swarms Descriptive Note Technical Report 06 Jul 2016 25 May 2017 Title OFFSETTING TOMORROW S ADVERSARY IN A CONTESTED ENVIRONMENT DEFENDING EXPEDITIONARY ADVANCE BASES IN 2025 AND BEYOND Descriptive Note Technical Report Title A Self Sustaining Solar Bio Nano Based Wastewater Treatment System for Forward Operating Bases Descriptive Note Technical Report 01 Feb 2012 31 Aug 2017 Title Radiation Hard and Self Healing Substrate Agnostic Nanocrystalline ZnO Thin Film Electronics Descriptive Note Technical Report 26 Sep 2011 25 Sep 2015 Title Modeling and Experiments with Carbon Nanotubes for Applications in High Performance Circuits Descriptive Note Technical Report Title Radiation Hard and Self Healing Substrate Agnostic

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