

AVR121: Enhancing ADC resolution by oversampling

Features

- Increasing the resolution by oversampling
- Averaging and decimation
- Noise reduction by averaging samples

1 Introduction

Atmel's AVR controller offers an Analog-to-Digital Converter with 10-bit resolution. In many cases 10-bit resolution is sufficient, but at some times higher accuracy is desired. Special signal processing techniques can be used to improve the resolution of the measurements. By using a method called "Oversampling and Decimation" higher resolution might be achieved without using an external ADC. This Application Note explains the method and which conditions need to be fulfilled to make this method work properly.

Figure 1-1: Enhancing the resolution



8-bit **AVR**
Microcontrollers

Application Note



Avr121 Enhancing Adc Resolution By Oversampling

Rodrigues, Joel J.P.C.



Avr121 Enhancing Adc Resolution By Oversampling:

Advanced Data Acquisition and Intelligent Data Processing Vladimir Haasz, Kurosh Madani, 2022-09-01 DAQ and data processing is a basic part of all automated production systems diagnostic systems watching over quality of production energy distribution transport control or in various other areas Demands on the speed accuracy and reliability increase in general It is possible to achieve not only using superior but also more expensive hardware but also applying advanced data acquisition and intelligent data processing It deals e g optimal data fusion of a number of sensors new stochastic methods for accuracy increasing new algorithms for acceleration of data processing etc These are the grounds for publishing this book *Advanced Data Acquisition and Intelligent Data Processing* offers 10 up to date examples of different applications of advanced data acquisition and intelligent data processing used in monitoring measuring and diagnostics systems The book arose based on the most interesting papers from this area published at IDAACS 2013 conference However the individual chapters include not only designed solution in wider context but also relevant theoretical parts achieved results and possible future ways Technical topics discussed in this book include advanced methods of data acquisition in application that are not routine measured data fusion using up to date advanced data processing nonlinear dynamical systems identification multidimensional image processing *Advanced Data Acquisition and Intelligent Data Processing* is ideal for personnel of firms deals with advanced instrumentation energy consumption monitoring environment monitoring non destructive diagnostics robotics etc as well as academic staff and postgraduate students in electrical control and computer engineering

Content

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Handbook of Modern Sensors Jacob Fraden, 2015-10-15 This book presents a comprehensive and up to date account of the theory physical principles design and practical implementations of various sensors for scientific industrial and consumer applications This latest edition focuses on the sensing technologies driven by the expanding use of sensors in mobile devices These new miniature sensors will be described with an emphasis on smart sensors which have embedded processing systems The chapter on chemical sensors has also been expanded to present the latest developments Digital systems however complex and intelligent they may be must receive information from the outside world that is generally analog and not electrical Sensors are interface devices between various physical values and the electronic circuits that understand only a language of moving electrical charges In other words sensors are the eyes ears

and noses of silicon chips Unlike other books on sensors the Handbook of Modern Sensors is organized according to the measured variables temperature pressure position etc This book is a reference text for students researchers interested in modern instrumentation applied physicists and engineers sensor designers application engineers and technicians whose job it is to understand select and or design sensors for practical systems **AVR Programming** Elliot Williams, 2014-01-27

Atmel s AVR microcontrollers are the chips that power Arduino and are the go to chip for many hobbyist and hardware hacking projects In this book you ll set aside the layers of abstraction provided by the Arduino environment and learn how to program AVR microcontrollers directly In doing so you ll get closer to the chip and you ll be able to squeeze more power and features out of it Each chapter of this book is centered around projects that incorporate that particular microcontroller topic Each project includes schematics code and illustrations of a working project Program a range of AVR chips Extend and re use other people s code and circuits Interface with USB I2C and SPI peripheral devices Learn to access the full range of power and speed of the microcontroller Build projects including Cylon Eyes a Square Wave Organ an AM Radio a Passive Light Sensor Alarm Temperature Logger and more Understand what s happening behind the scenes even when using the Arduino IDE **Emerging Communication Technologies for E-Health and Medicine** Rodrigues, Joel J.P.C., 2012-04-30

According to the World Health Organisation WHO e health is the combined use of electronic communication and information technology in the health sector and moreover it enables a safer higher quality more equitable and sustainable health system Emerging Communication Technologies for E Health and Medicine is a fundamental source for the advancement of knowledge application and practice in the interdisciplinary areas of healthcare e health m health u health sensors biomedical engineering and telemedicine Due to its grounding in research and theory evidence this book is designed for use in graduate courses in health management medicine nursing health professionals and medical informatics The book can help to e health contents applications and interesting experiences It is an important way to communicate e health concepts *Avr E*

Arduino: Técnicas De Projeto Charles Borges De Lima E Marco V. M. Villação, 2012-05-30 Devido ao seu desempenho os microcontroladores AVR t m assumido um papel de destaque entre os microcontroladores de 8 bits Sua arquitetura moderna al m de permitir execu es mais r pidas dos programas permite uma maior densidade de c digo comparado s outras tecnologias de 8 bits A plataforma Arduino tornou populares os microcontroladores AVR possibilitando que esses alcancem um n mero cada vez maior de pessoas A plataforma Arduino associa principalmente a facilidade de programa o com a disponibilidade de in meros perif ricos na forma de m dulos ferramentas de programa o gratuitas e amplo suporte t cnico Ao abordar a tecnologia AVR voltada ao emprego da plataforma Arduino com o ATmega328 esta obra inclui in meras t cnicas para o projeto de sistemas microcontrolados raramente encontradas em um nico livro tais como o uso de displays LCD alfanum ricos e gr ficos gera o de m sicas curtas leitura de teclado matriz e cubo de LEDs t cnicas de multiplexa o gera o de formas de onda comunica o serial com um computador comunica o sem fio cart es de mem ria sonar leitura de sensores

acionamento de motores conversores CC/CC e CC/CA além de um grande conjunto de programas com técnicas de programação incluindo aplicação portando um Sistema Operacional de Tempo Real RTOS. Apresenta também as técnicas para o desenho de placas de circuito impresso e o projeto de chaves transistorizadas. Inclui ainda a apresentação de um software para a simulação de microcontroladores de fácil e crescente uso nos meios acadêmico e industrial o Proteus ISIS que permite a simulação dos circuitos apresentados. Os inúmeros programas desenvolvidos contam com seus respectivos códigos em linguagem C os quais podem ser empregados para qualquer outra tecnologia de microcontroladores devido portabilidade dessa linguagem. Ao final de cada assunto são sugeridos exercícios que além de apresentarem ideias de projeto apresentam as informações técnicas necessárias permitindo o aperfeiçoamento crescente e a solidificação do conhecimento. Em resumo esta obra apresenta uma abordagem objetiva e prática para o ensino profissional de inúmeras técnicas de projeto aplicado aos microcontroladores incluindo a teoria básica que proporciona a compreensão e o aprendizado dos projetos. **Design News**, 2008

High-performance Oversampling A/D Converter Design Techniques in Scaled CMOS Technologies Shaolan Li, 2018

Oversampling analog to digital converters ADCs are specialists in digitizing real world signals in high resolution. They have been crucial building blocks in many modern electronic systems and are expected to have a growing significance in the booming era of Internet of Things IoT. However many classic oversample ADC techniques are power hungry and scaling unfriendly making them deficient for many emerging applications. To address this challenge this thesis explores solution from two directions voltage controlled oscillator VCO based ADC and hybrid ADC. The first work presents a VCO based ADC featuring a novel phase extended quantizer PEQ. Compared to prior VCO based ADCs the proposed phase extension technique enabled this work to achieve 1 bit higher resolution with very little power and circuit overhead. On top of resolution boosting a tri-level resistor digital to analog converter DAC is also introduced as complementary to the new quantizer enabling high DR while creating a dynamic power saving mechanism for the proposed design. Fabricated in 130 nm CMOS the prototype ADC achieved peak Schreier Figure of Merits FoM of 174.3 dB marking 2.5x improvement over prior arts. The second project extends the achievement of the first and develops techniques to push the performance frontier of high order VCO based ADC. Existing high order VCO based ADCs still rely on OTA based active loop filter which deemphasizes the merits of the VCO based quantizer. To address their limitation a hybrid passive VCO architecture is proposed where we made the front end loop filter fully passive and zero power and used the VCO to support the entire loop gain. This technique innovatively utilizes the parasitic effect of the VCO hence also obviates the need for parasitic cancellation. A prototype fabricated in 40 nm CMOS measured 19 fJ conversion Walden FoM achieving 5x improvement over existing high order VCO based ADC. Finally this thesis also presents the design of a noise shaping SAR/NS SAR ADC. Unlike prior works that all rely on the cascaded integrator feed forward CIFF structure this work distinctively employs the error feedback EF structure. It is the first in its kind to achieve second order NTF with complex zero optimization using all low

power scaling friendly building blocks such as passive finite impulse response FIR filter and dynamic amplifier D Amp A background calibration scheme is also developed to improve robustness over process voltage temperature PVT variation The prototype chip fabricated in 40nm CMOS measured the state of the art performance of 178 dB Schreier FoM This work demonstrated a NS SAR solution that combines optimized NTF power efficiency and PVT robustness *Oversampling A/D Converters with Improved Signal Transfer Functions* Bupesh Pandita,2011-09-15 This book describes techniques for designing complex discrete time ADCs with signal transfer functions that significantly filter interfering signals The book provides an understanding of theory issues and implementation of discrete complex ADCs The concepts developed in each chapter are further explained by applying them to a target application of ADCs in DTV receivers **Faster Scaling for Oversampling ADC's** Bashar H. Atiyat,2003 *Binary Dithered Oversampling Analog-to-digital Converters* Diego Pienovi,2009 In today's world analog to digital converters ADC play a major role Our modern society requires and depends on electronic devices that process the analog input data in the digital domain such as cellphones audio and video systems and even domestic appliances Therefore the development of fast and accurate ADCs have become a key issue for the industry In general a good ADC is the one that achieves high resolution low quantization noise with low complexity One of the most popular techniques to decrease the quantization noise is to digitalize the incoming signal with a sampling frequency many times higher than twice the signal bandwidth This technique is called oversampling Probably the most popular oversampling converters are the Sigma Delta SD modulators which use a very high sampling frequency and a binary quantizer for first order SD In SD the quantizer is embedded into a feedback loop in such a way that the quantization noise is not only spread over the spectrum because of oversampling but it is also shaped to the upper frequencies this is called noise shaping The big problem with SD is that the quantization noise spectrum presents undesired harmonics caused by the nonlinear nature of the quantizer To avoid this the solution is to add an independent signal before the quantization stage called dither It was proven by Lipshitz and Vanderkooy in 1 that dithering a first order SD modulator is ineffective as it turns the modulator in constant overload In addition to this problem because of the feedback loop higher order SD modulators can be unstable That being said the aim of this work is to present a simple oversampling ADC without feedback capable of generating the minimum uncorrelated quantization noise that yields the maximum possible SNR at the output For that purpose this work develops the statistical characteristics of the optimum dither that achieves the mentioned goal for different types of input signals

Power-Efficient High-Speed Parallel-Sampling ADCs for Broadband Multi-carrier Systems Yu Lin,Hans Hegt,Kostas Doris,Arthur H.M. van Roermund,2015-05-07 This book addresses the challenges of designing high performance analog to digital converters ADCs based on the smart data converters concept which implies context awareness on chip intelligence and adaptation Readers will learn to exploit various information either a priori or a posteriori obtained from devices signals applications or the ambient situations etc for circuit and architecture optimization during the design phase or

adaptation during operation to enhance data converters performance flexibility robustness and power efficiency The authors focus on exploiting the a priori knowledge of the system application to develop enhancement techniques for ADCs with particular emphasis on improving the power efficiency of high speed and high resolution ADCs for broadband multi carrier systems

A Background Digital Calibration Technique for Oversampling Delta/Sigma Analog to Digital

Converters with 2-bit Internal Quantizers José S. Niell,1995

Resolution Enhancement of Analog-to-digital Converters Through Computationally Simple Digital Filtering Eric L. Zahl,1989

The resolution of analog to digital converters can be distinguished as absolute resolution or average resolution This study reviews average resolution enhancement techniques and proposes a method which is particularly applicable as a low cost modification to a high speed waveform acquisition system This method uses oversampling combined with computationally simple digital filtering to enhance the average resolution of an analog to digital A D converter while maintaining an absolute resolution which is at least that of the unmodified system The average resolution enhancement is approximately $1.2 \log_2 N$ bits where N is the oversampling ratio The simple digital filter is also shown to be useful in reducing alias errors when sample rates are reduced to near Nyquist rates Additive dither signals are shown to be useful in maintaining expected resolution enhancement for certain input signals

A Prototype of a New Class of Oversampling ADC Jun He,2006 Analog to digital A D and digital to analog D A converters are important blocks in signal processing system because they provide the link between the analog world and digital systems Compared with Nyquist rate data converters oversampling data converters are more desirable for modern submicron technologies with low voltage supplies Today all existing oversampling modulators in popular use are derived from sigma delta modulation Stability is the most significant problem in the sigma delta modulator because the ultimate accuracy is limited by stability As the aggressiveness of the design increases the margin of stability diminishes rapidly This thesis presents the design and experimental results of the first prototype circuit implementation of the novel oversampling modulation scheme proposed by Dr Takis Zourntos This new class of oversampling modulators are theoretically stable With less stability limitation the new class of modulators can potentially achieve higher signal to noise ratio SNR or less power by designing the modulator more aggressively This thesis describes the methods and procedures of how the new oversampling modulation theory is implemented into a circuit Some novel circuit architectures are proposed in this modulator such as a filter which can provide status outputs for the controller and realize arbitrary zeros and poles comparators with synchronization latches to eliminate the effect of metastability and a digital to analog converter DAC with current calibration circuits for high linearity A third order continuous time oversampling modulator employing 4 bit quantization is implemented in a $0.35 \mu\text{m}$ double poly complementary metal oxide semiconductor CMOS technology with a chip area of $2150 \times 2150 \mu\text{m}^2$ Simulation results show it achieves 83.7 dB peak SQNR 90 dB dynamic range over a 500kHz input signal bandwidth and 60 mW power consumption

Low-voltage, Low-power, High-resolution, Broadband

Oversampling Analog-to-digital Conversion Je-Kwang Cho, 2012

Oversampling A/D converters exchange resolution in time for that in amplitude by oversampling the input signal and employing sigma delta modulators that suppress quantization error within the signal bandwidth. As a result, a high precision A/D converter output can be generated by using back end digital decimation filtering. However, the use of oversampling converters is typically limited to low bandwidth applications such as digital audio systems. Recently, sigma delta modulators operating at relatively low oversampling ratios have been shown to be effective at achieving high performance A/D conversion for signal bandwidths of several megahertz. However, the limited signal swings and voltage headroom that accompany the aggressive scaling of CMOS technology result in high power dissipation of the analog circuits in conventional modulator architectures. Although sigma delta modulators based on input feedforward architectures enable reduced analog power dissipation, they require a high speed quantizer and feedback DAC with attendant high power dissipation. The objective of this research is to investigate means of power minimization for both analog and digital circuits in sigma delta modulators operating from low supply voltages over several megahertz of signal bandwidth while maintaining high precision. To relax the timing constraints on the quantizer and feedback DAC, a half sample delayed input feedback architecture is employed in the implementation of a second order sigma delta modulator. Power dissipation in the analog amplifiers of the feedforward architecture is reduced by using a single amplifier to implement the two integrators. This amplifier sharing also reduces the area occupied by the integrators. The power scaling of amplifiers in discrete time multi order amplifier based analog integrators is exploited by dynamically biasing the shared amplifier. A low power high speed charge pump circuit for dynamic biasing minimizes the power overhead. Finally, a multi bit quantizer which effectively reduces the output amplitude and power dissipation of the integrators employs interpolated preamplifiers to conserve power and area in the preamplifiers. A 2/2 cascaded sigma delta modulator operating from a 1.0 V supply has been designed using a half sample delayed input feedforward architecture for each stage, dynamically biased amplifier sharing for realization of the integrators, and interpolated multi bit quantization. An experimental prototype of the proposed modulator has been integrated in a 0.18 micrometer CMOS technology. At a 40 MHz sampling rate, the prototype achieves 92 dB of dynamic range, a 91 dB peak SNR, and an 84 dB peak SNDR for a signal bandwidth of 1.25 MHz while consuming only 24.3 mW of total power from a 1.0 V supply.

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