

Design and Verification of AXI OCP Bridge Supporting Out-of-Order Transactions for achieving Dead Lock Free Communication

Author(s) Name: Shrikant, Roopa K.
Bangalore, Karnataka

Abstract—Modern on-chip communication protocols such as advanced eXtensible Interface and open core protocol support advanced transactions to improve communication efficiency. Out-of-order transactions that allow responses to be returned in an order different from their request order play an important role in this improvement. However, a deadlock situation may occur if these transactions are not properly manipulated. In this paper, we address the deadlock problem in an on-chip bus system supporting out-of-order transactions. We present a graphic model that can well represent the status of a bus system and show that a cycle exists in the graph if and only if the bus system is in an unsafe state that may lead to a bus deadlock. Based on this model, we propose a novel bus design technique that can efficiently resolve the bus deadlock problem. Experimental result show that buses with the proposed technique can be up to 3.3 times faster than those with the currently available techniques.

Index Terms—Advanced eXtensible Interface (AXI), bus deadlock, on-chip bus, open core protocol (OCP), out-of-order execution, tagged transactions.

I. INTRODUCTION

In the past decade, the advanced high-performance bus and advanced peripheral bus of advanced microcontroller bus architecture [1] are the most popular communication architectures for SOC designs. Both architectures are shared-link buses allowing only one master IP to access one slave IP at a time. Recently, the communication efficiency of shared link buses becomes insufficient because of their lack of parallel access capability. Some more advanced communication protocols such as advanced eXtensible Interface (AXI) [1] and open core protocol (OCP) [2] that facilitate parallel communication are thus proposed. Both AXI and OCP define communication interface protocols and transaction types but leave communication architecture to interconnect designers. Interconnect designers thus have the freedom to implement the communication protocols using multilayer, crossbar, networks-on-chip [3], or a combination of these designs to increase the communication parallelism. The communication protocols defined in AXI and OCP support various advanced transactions, including burst transactions, pipelined (outstanding) transactions, and out-of-order transactions [1], [2]. Among these transactions, the out-of-order transactions serve as a major key to improve system performance. Out-of-order transactions can be executed more efficiently when a master IP, such as a processor, can handle out-of-order returns as it allows a slave core such as a dynamic random-access memory controller to service requests in the order that is most convenient, rather than the order in which requests are sent by the master [2]. In [4] and [5], the authors show that by employing out-of-order mechanisms in memory controllers, the average execution time can be reduced by 21% to 41% over the conventional in-order memory accessing. Bus deadlock is a problem that

occurs when a set of IP cores communicating through a bus system are involved in a circular wait-and-hold state that cannot be resolved. This problem may crash a bus system as none of the IP cores involved in the deadlock can continue its functions. In [6], the authors invest the bus deadlock problem of a system that allows a master to execute a process only if the master is granted to access all required slaves of the process and each master will hold the slaves granted to it until all its required slaves are granted to it. A bus deadlock happens when each master in a set of masters is holding a slave and waiting for another slave held by another master in the set. In this type of bus deadlocks, the relation between masters and slaves is similar to that between processes and resources in an operating system (OS) where a deadlock occurs when there is a circular wait-and-hold relation among a set of processes and resources [7]. A resource allocation graph (RAG) is commonly utilized to represent the status of resource allocation in an OS [7]. A vertex in a RAG represents a process or a resource. A directed edge from a process vertex to a resource vertex denotes that the process is requesting the resource, and one from a resource vertex to a process vertex denotes that the resource is being held by the process. In an OS, a deadlock may occur when a cycle exists in the RAG [7]. In [6], the authors thus map the bus deadlock problem to the OS deadlock problem and propose a hardware approach which requires two to four clock cycles to detect the occurrence of a bus deadlock. In advanced bus/interface protocols such as AXI and OCP, a slave must return responses after some latency when it accepts a transaction request from a master. After the responses are returned and accepted, the transaction is completed and the slave must be released. As a result, a slave will be released from a master no matter whether the master is granted to access all its required slaves or not and thus the bus deadlock problem described in [6] does not happen in these protocols. However, another type of bus deadlock may occur because of the out-of-order transactions supported by these protocols. This is because in general a bus system supporting out-of-order transactions also needs to support transactions that do not allow out-of-order execution. For example, a read operation must wait for a preceding write operation if they address to the same memory location. Such read-after-write operations are commonly encountered in a bus system and they clearly do not allow out-of-order execution. To distinguish the transactions allowing and not allowing out-of-order, both AXI and OCP protocols define tagged transactions, in which a master tags an ID to each transaction in the way that the transactions whose responses must be returned in order are tagged with the same ID. A bus that fully supports the AXI or OCP protocol is responsible for assuring that the order of the responses returned to each master is the same as their request order if they have the same ID. Thus, the response returned by a slave may not be accepted by the bus and the slave has to wait until the order violation condition disappears. As a tagged transaction must wait for the completion of an earlier issued transaction with the same ID, it is possible that a set

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Proceedings of the 5th International Conference on Frontiers in Intelligent Computing: Theory and Applications Suresh Chandra Satapathy, Vikrant Bhateja, Siba K. Udgata, Prasant Kumar Pattnaik, 2017-03-02 The book is a collection of high quality peer reviewed research papers presented at International Conference on Frontiers of Intelligent Computing Theory and applications FICTA 2016 held at School of Computer Engineering KIIT University Bhubaneswar India during 16 17 September 2016 The book aims to present theories methodologies new ideas experiences applications in all areas of intelligent computing and its applications to various engineering disciplines like computer science electronics electrical mechanical engineering etc *Reconfigurable Computing: Architectures, Tools, and Applications* Diana Goehringer, Marco Domenico Santambrogio, João M.P. Cardoso, Koen Bertels, 2014-04-09 This book constitutes the thoroughly refereed conference proceedings of the 10th International Symposium on Reconfigurable Computing Architectures Tools and Applications ARC 2014 held in Vilamoura Portugal in April 2014 The 16 revised full papers presented together with 17 short papers and 6 special session papers were carefully reviewed and selected from 57 submissions The topics covered are applications methods frameworks and OS for debug over clocking and relocation memory architectures methodologies and tools and architectures Advances in Communication, Devices and Networking Rabindranath Bera, Subir Kumar Sarkar, Om Prakash Singh, Hemanta Saikia, 2019-02-15 The book covers recent trends in the field of devices wireless communication and networking It presents the outcomes of the International Conference in Communication Devices and Networking ICCDN 2018 which was organized by the Department of Electronics and Communication Engineering Sikkim Manipal Institute of Technology Sikkim India on 2 3 June 2018 Gathering cutting edge research papers prepared by researchers engineers and industry professionals it will help young and experienced scientists and developers alike to explore new perspectives and offer them inspirations on addressing real world problems in the field of electronics communication devices and networking On-Chip Communication Architectures Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication

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Communication Architectures for Systems-on-Chip José L. Ayala, 2018-09-03 A

presentation of state of the art approaches from an industrial applications perspective Communication Architectures for Systems on Chip shows professionals researchers and students how to attack the problem of data communication in the manufacture of SoC architectures With its lucid illustration of current trends and research improving the performance quality and reliability of transactions this is an essential reference for anyone dealing with communication mechanisms for embedded systems systems on chip and multiprocessor architectures or trying to overcome existing limitations Exploring architectures currently implemented in manufactured SoCs and those being proposed this book analyzes a wide range of applications including Well established communication buses Less common networks on chip Modern technologies that include the use of carbon nanotubes CNTs Optical links used to speed up data transfer and boost both security and quality of service QoS The book's contributors pay special attention to newer problems including how to protect transactions of critical on chip information personal data security keys etc from an external attack They examine mechanisms revise communication protocols involved and analyze overall impact on system performance

Embedded Systems Handbook 2-Volume Set

Richard Zurawski, 2018-10-08 During the past few years there has been an dramatic upsurge in research and development implementations of new technologies and deployments of actual solutions and technologies in the diverse application areas of embedded systems These areas include automotive electronics industrial automated systems and building automation and control Comprising 48 chapters and the contributions of 74 leading experts from industry and academia the Embedded Systems Handbook Second Edition presents a comprehensive view of embedded systems their design verification networking and applications The contributors directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews exploring new developments deployments and trends To accommodate the tremendous growth in the field the handbook is now divided into two volumes New in This Edition Processors for embedded systems Processor centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections It begins with a brief introduction to embedded systems design and verification The book then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Networked Embedded Systems Volume

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Design and Verification of Bus Bridge from Ocp to AHB Ranganathan Sundaram, 2012. Protocols are commonly used to connect IP blocks on structured SoCs. Generally, Protocol is the back bone of the SoC and its failure usually leads to a non functional chip. In present market various types of standard protocols are available and are used in SoC which requires a bridge to pass the information from one type of protocol to other type of protocol safely and without any data loss. OCP and AMBA AHB protocol are commonly used protocols. In this work the bus bridge has been designed to interface these protocols which plays a vital role in SoC application such as it may lead to application failure if it doesn't work properly. Initially OCP and AHB protocols are modeled separately using VHDL and are simulated. Basically Bus Bridge should convert command and data of OCP formats to acceptable AHB formats. This conversion does not ensure proper communication unless the timings of each protocol were met. Hence the interconnecting Bus Bridge wrapper between Core Centric Protocol OCP and Bus Centric Protocol AHB was designed with proper timing delay. Also the PSL assertions are written in order to verify the behavior of protocols.

Design Verification and Performance Analysis of Serial AXI Links in Broadcom System-on-Chip Simran Kaur Sarai, 2014. Design verification is an essential step in the development of any product. Also referred to as qualification testing, design verification ensures that the product as designed is the same as the product as intended. In this project design verification and performance analysis of Thin Advanced Extensible Interface Links T AXI is conducted on a Broadcom's SoC System on Chip. T AXI is a Broadcom's proprietary bus that interfaces all the subsystems on the System onchip SoC to the system memory. Test cases are developed to verify the functionality of the T AXI and performance verification is implemented using scenarios derived from real world examples. A Field Programmable Gate Array FPGA is used to emulate the SoC design and C programming is used to write the test cases. The test results verify the T AXI functionality and the performance analysis supports the theoretical calculations.

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