

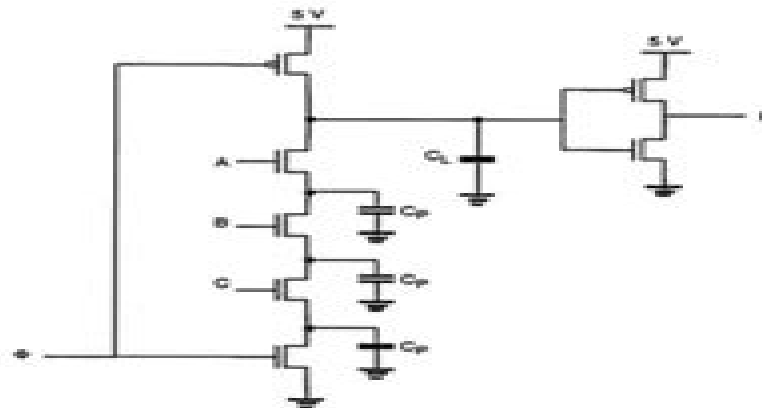


Figure P9.6

SOLUTION:

The total charge at node C_L before charge sharing is

$$Q_L = V_{in} \cdot C_L = 5C_L$$

After charge sharing, suppose the node voltage is V_{final} , then

$$Q_L = 5C_L = V_{final} \cdot C_L + V_{final} \cdot C_P$$

To prevent the inverter from switching,

$$V_{final} = \frac{5C_L}{C_L + C_P} > 3$$

The maximum ratio is:

$$\frac{C_P}{C_L} < \frac{2}{3}$$

9.7 Consider the following CMOS logic circuit which is a simple domino circuit. Node X is connected to a CMOS inverter so that the output of the inverter can be directly fed to the next stage of the domino circuit.

- (a) Explain how the voltage level at node X, after it is precharged to 5 V, can be affected by the charge sharing between node X and node Y if their node capacitances are the same. Express the final voltage at node X in terms of the initial voltage at node Y when the charge sharing is completed following the full precharge operation when the gate terminal of M2 transistor is fixed at 0 V.

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Engineering

Education, 1989 **Embedded SoPC Design with Nios II Processor and Verilog Examples** Pong P. Chu, 2012-05-14

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Introduction to VLSI Systems Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration

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Digital Integrated Electronics [with] Solutions Manual Herbert Taub,1977

Automatic Analog IC Sizing and Optimization Constrained with PVT Corners and Layout Effects Nuno Lourenço,Ricardo Martins,Nuno Horta,2016-07-29 This book introduces readers to a variety of tools for automatic analog integrated circuit IC sizing and optimization The authors provide a historical perspective on the early methods proposed to tackle automatic analog circuit sizing with emphasis on the methodologies to size and optimize the circuit and on the methodologies to estimate the circuit s performance The discussion also includes robust circuit design and optimization and the most recent advances in layout aware analog sizing approaches The authors describe a methodology for an automatic flow for analog IC design including details of the inputs and interfaces multi objective optimization techniques and the enhancements made in the base implementation by using machine learning techniques The Gradient model is discussed in detail along with the methods to include layout effects in the circuit sizing The concepts and algorithms of all the modules are thoroughly described enabling readers to reproduce the methodologies improve the quality of their designs or use them as starting point for a new tool An extensive set of application examples is included to demonstrate the capabilities and features of the methodologies described

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