FPGA INTERVIEW QUESTIONS

What is FPGA?

A field-programmable gate array is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function—hence the name "field-programmable". FPGAs are usually slower than their application-specific integrated circuit (ASIC) counterparts, cannot handle as complex a design, and draw more power (for any given semiconductor process). But their advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The designs are developed on regular FPGAs and then migrated into a fixed version that more resembles an ASIC.

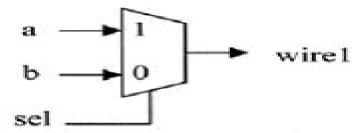
What logic is inferred when there are multiple assign statements targeting the same wire?

It is illegal to specify multiple assign statements to the same wire in a synthesizable code that will become an output port of the module. The synthesis tools give a syntax error that a net is being driven by more than one source. However, it is legal to drive a three-state wire by multiple assign statements.

What do conditional assignments get inferred into?

Conditionals in a continuous assignment are specified through the "?" operator. Conditionals get inferred into a multiplexor. For example, the following is the code for a simple multiplexor.

assign wire! = (sel==1%1) ? a : b;



What value is inferred when multiple procedural assignments made to the same reg variable in an always block?

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unsuccessful interviews we thought of writing a book to help upcoming undergrads and experience professionals to get selected in such interviews The book covers every dimension related to FPGA Verilog STA and Protocols In simple words don t search anything on the internet this book is the Google of FPGA and Verilog Proceedings, 1997 **EDN**, 2009

ASIC and FPGA Verification Richard Munden, 2004-10-23 Richard Munden demonstrates how to create and use simulation models for verifying ASIC and FPGA designs and board level designs that use off the shelf digital components Based on the VHDL VITAL standard these models include timing constraints and propagation delays that are required for accurate verification of today s digital designs ASIC and FPGA Verification A Guide to Component Modeling expertly illustrates how ASICs and FPGAs can be verified in the larger context of a board or a system It is a valuable resource for any designer who simulates multi chip digital designs Provides numerous models and a clearly defined methodology for performing board level simulation Covers the details of modeling for verification of both logic and timing First book to collect and teach techniques for using VHDL to model off the shelf or IP digital components for use in FPGA and board level design Quantifying and Exploring the Gap Between FPGAs and ASICs verification **Business Periodicals Index** ,2000 Ian Kuon, Jonathan Rose, 2010-07-03 Field programmable gate arrays FPGAs which are pre fabricated programmable digital integrated circuits ICs provide easy access to state of the art integrated circuit process technology and in doing so democratize this technology of our time This book is about comparing the qualities of FPGA their speed performance area and power consumption against custom fabricated ICs and exploring ways of mitigating their de ciencies This work began as a guestion that many have asked and few had the resources to answer how much worse is an FPGA compared to a custom designed chip As we dealt with that question we found that it was far more dif cult to answer than we anticipated but that the results were rich basic insights on fundamental understandings of FPGA architecture It also encouraged us to nd ways to leverage those insights to seek ways to make FPGA technology better which is what the second half of the book is about While the question How much worse is an FPGA than an ASIC has been a constant sub theme of all research on FPGAs it was posed most directly some time around May 2004 by Professor Abbas El Gamal from Stanford University to us he was working on a 3D FPGA and was wondering if any real measurements had been made in this kind of comparison Shortly thereafter we took it up and tried to answer in a serious way Gateway to VLSI Bharat Agarwal, Kshitij Goel, 2019-10-04 If you can spare half an hour then we can guarantee success at your next VLSI Very Large Scale Integration FPGA Field Programmable Gate Array STA Static Timing analysis interview Do you want to secure at least 3 to 4 job offers by succeeding at all the phone and on site job interviews for the FPGA DESIGN ENGINEER position Or do you simply want answers for the most frequently asked interview questions in VLSI FPGA digital circuit design Did you know that people who target question answer type preparation for a job interview are 3 4 times more likely to get a job offer than those who don t Did you also know that there is a set of questions that is likely to be repeatedly asked by interviewers across the industry no matter who

you talk with in the VLSI FPGA digital design After a total of 17 unsuccessful interviews we thought of writing a book to help upcoming undergrads and experience professionals to get selected in such interviews The book covers every dimension related to FPGA Verilog STA and Protocols In simple words don t search anything on the internet this book is the Google of ASIC Design and Synthesis Vaibbhav Taraate, 2021-01-06 This book describes simple to complex ASIC design practical scenarios using Verilog It builds a story from the basic fundamentals of ASIC designs to advanced RTL design concepts using Verilog Looking at current trends of miniaturization the contents provide practical information on the issues in ASIC design and synthesis using Synopsys DC and their solution The book explains how to write efficient RTL using Verilog and how to improve design performance It also covers architecture design strategies multiple clock domain designs low power design techniques DFT pre layout STA and the overall ASIC design flow with case studies The contents of this book will be useful to practicing hardware engineers students and hobbyists looking to learn about ASIC design and synthesis Tree-based Heterogeneous FPGA Architectures Umer Faroog, Zied Marrakchi, Habib Mehrez, 2012-05-17 This book presents a new FPGA architecture known as tree based FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures HDL Based ASIC and FPGA Design Methodology Using **Synopsys and Xilinx** Igbalur R. Rokan, 1997 FPGA -Based Systems Design and Practice Ming-Bo Lin, 2018-07-30 With the advance of semiconductor and communication industry the use of system on chip SoC has become an essential technique to reduce product costs The development of a good understanding of the key stages of the hardware description language HDL design flow based on cell based libraries or field programmable gate array FPGA devices becomes essential This book addresses the needs for such a topic based on Verilog HDL and FPGAs The most important features of this book include HDL based design has become an essential technique for modern digital systems. This book focuses on developing verifying and synthesizing designs of practical digital systems using the most widely used hardware description Language Verilog HDL and FPGAs The main features of this book include Explaining how to perform synthesis and verification to achieve optimized synthesis results and compiler times Illustrating the entire design and verification flow using an FPGA case study Emphasizing design implementation trade off options with coverage of ASICs and FPGAs Providing plentiful worked examples and review questions in each section for readers to test their understanding of the related topics Giving readers deeper understanding with plentiful review questions in each section and end of chapter problems Incorporating many case studies to help the reader grasp the essentials of practical digital systems to be designed using Verilog HDL and FPGAs Highlighting Verilog HDL syntax throughout the book to facilitate readers to refer the desired syntax as they need Printing all keywords in boldface throughout the book to emphasize the language structures and improve the readability of

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