

Parameters

System: kipro_sin_cos Path: CORDIC_0

ALTERA_CORDIC

altera_cordic

Details

Functionality Performance

Function

Name: Sin Cos

Input Data Widths

Fraction: 10 bits
Width: 13 bits
Sign: signed

Output Data Widths

Fraction: 8 bits
Width: 10 bits
Sign: signed

Ports

☐ Generate an enable port

Details Block Symbol

ALTERA_CORDIC

Name altera_cordic
Version 20.1
Author Altera Corporation

A collection of fixed point Basic Functions/Arithmetic

https://documentation.altera.com/#/doc/topic/v19_1/cordic_0.html
https://documentation.altera.com/#/doc/topic/v19_1/cordic_0.html

Generate Completed

All

Progress: Adding CORDIC_0 [altera_cordic 20.1]
Progress: Parameterizing module CORDIC_0
Progress: Building connections
Progress: Parameterizing connections
Progress: Validating
Progress: Done reading input file
Info: kipro_sin_cos: Generating kipro_sin_cos "kipro_sin_cos" for QUARTUS_SYNTH
Info: CORDIC_0: C:\IntelFPGA_Ite\20.1\quartus\libra/backend/windows64/condPolyEval -target Cyclone6
Error: CORDIC_0: Could not generate name
Error: CORDIC_0: Failed to generate HDL for current parameters
Warning: CORDIC_0: Cannot Achieve Frequency at any possible latency
Warning: CORDIC_0: Unable to estimate resource usage
Error: add_filesset_file: file such file C:\Users\KIPRAS\AppData\Local\Temp\alt8519_71.
Info: CORDIC_0: "kipro_sin_cos" instantiated altera_cordic "CORDIC_0"
Info: kipro_sin_cos: Done "kipro_sin_cos" with 2 modules, 3 files
Error: qsys-generate failed with exit code 1: 3 Errors, 2 Warnings
Info: Finished: Create HDL design files for synthesis

Generate: completed with errors and warnings.

Finish Close

Messages

Type	Path	Message
------	------	---------

Altera High Definition Multimedia Interface Ip Core User Guide

**Xin-She Yang, Simon Sherratt, Nilanjan
Dey, Amit Joshi**



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