

SECOND EDITION

DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE

JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ

Unique in approach, this text offers comprehensive coverage of new design methodologies and implementation strategies of digital ICs and brings to the forefront a number of new issues that impact the reliability, cost, performance, and power dissipation of chips now reaching the 100-nm realm. This means increased importance in circuit design of deep submicron transistor effects, interconnect, signal integrity, high-performance and low-power design, timing and clock distribution. In contrast to the first edition, the present text focuses entirely on CMOS ICs. While introducing these changes, the text preserves the spirit and goals of the first edition—that is, it successfully bridges the gap between the circuit and system visions on digital design.

Beginning with solid discussions on the operation of electronic devices and in-depth analysis of the nucleus of digital design—the inverter—the text gradually channels this knowledge into the design of more complex modules such as gates, controllers, adders, multipliers, and memories. Actual design examples and layouts are interspersed throughout the text. Besides numerous examples, each chapter also contains a number of problems or brain teasers that provoke thinking and understanding while reading. Fully worked-out design problems are available from the web site: (<http://bwrc.eecs.berkeley.edu/icBook>).

The text is intended for use in digital circuit design courses conducted for undergraduate and postgraduate students of electronics.



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Digital Integrated Circuits Jan M. Rabaey, 2003 Contents p pChapter 1 Introductionp pChapter 2 The Manufacturing Processp pChapter 3 The Devicesp pChapter 4 The Wirep pChapter 5 The CMOS Inverterp pChapter 6 Designing Combinational Logic Gates in CMOS **Digital Integrated Circuits** Jan M. Rabaey, 2003 *Split Manufacturing of Integrated Circuits for Hardware Security and Trust* Ranga Vemuri, Suyuan Chen, 2021-05-25 Globalization of the integrated circuit IC supply chains led to many potential vulnerabilities Several attack scenarios can exploit these vulnerabilities to reverse engineer IC designs or to insert malicious trojan circuits Split manufacturing refers to the process of splitting an IC design into multiple parts and fabricating these parts at two or more foundries such that the design is secure even when some or all of those foundries are potentially untrusted Realizing its security benefits researchers have proposed split fabrication methods for 2D 2.5D and the emerging 3D ICs Both attack methods against split designs and defense techniques to thwart those attacks while minimizing overheads have steadily progressed over the past decade This book presents a comprehensive review of the state of the art and emerging directions in design splitting for secure split fabrication design recognition and recovery attacks against split designs and design techniques to defend against those attacks Readers will learn methodologies for secure and trusted IC design and fabrication using split design methods to protect against supply chain vulnerabilities *CMOS Circuits for Passive Wireless Microsystems* Fei Yuan, 2010-10-28 This book provides a comprehensive treatment of CMOS circuits for passive wireless microsystems Major topics include an overview of passive wireless microsystems design challenges of passive wireless microsystems fundamental issues of ultra low power wireless communications radio frequency power harvesting ultra low power modulators and demodulators ultra low power temperature compensated current and voltage references clock generation and remote calibration and advanced design techniques for ultra low power analog signal processing *Advanced Circuits for Emerging Technologies* Krzysztof Iniewski, 2012-04-17 The book will address the state of the art in integrated circuit design in the context of emerging systems New exciting opportunities in body area networks wireless communications data networking and optical imaging are discussed Emerging materials that can take system performance beyond standard CMOS like Silicon on Insulator SOI Silicon Germanium SiGe and Indium Phosphide InP are explored Three dimensional 3D CMOS integration and co integration with sensor technology are described as well The book is a must for anyone serious about circuit design for future technologies The book is written by top notch international experts in industry and academia The intended audience is practicing engineers with integrated circuit background The book will be also used as a recommended reading and supplementary material in graduate course curriculum Intended audience is professionals working in the integrated circuit design field Their job titles might be design engineer product manager marketing manager design team leader etc The book will be also used by graduate students Many of the chapter authors are University Professors *Micro-Relay Technology for*

Energy-Efficient Integrated Circuits Hei Kam, Fred Chen, 2014-10-16 This volume describes the design of relay based circuit systems from device fabrication to circuit micro architectures This book is ideal for both device engineers as well as circuit system designers and highlights the importance of co design across design hierarchies when trying to optimize system performance in this case energy efficiency The book will also appeal to researchers and engineers focused on semiconductor integrated circuits and energy efficient electronics

Flip-Flop Design in Nanometer CMOS Massimo Alioto, Elio Consoli, Gaetano Palumbo, 2014-10-14 This book provides a unified treatment of Flip Flop design and selection in nanometer CMOS VLSI systems The design aspects related to the energy delay tradeoff in Flip Flops are discussed including their energy optimal selection according to the targeted application and the detailed circuit design in nanometer CMOS VLSI systems Design strategies are derived in a coherent framework that includes explicitly nanometer effects including leakage layout parasitics and process voltage temperature variations as main advances over the existing body of work in the field The related design tradeoffs are explored in a wide range of applications and the related energy performance targets A wide range of existing and recently proposed Flip Flop topologies are discussed Theoretical foundations are provided to set the stage for the derivation of design guidelines and emphasis is given on practical aspects and consequences of the presented results Analytical models and derivations are introduced when needed to gain an insight into the inter dependence of design parameters under practical constraints This book serves as a valuable reference for practicing engineers working in the VLSI design area and as text book for senior undergraduate graduate and postgraduate students already familiar with digital circuits and timing

Analog Circuit Design Michiel Steyaert, Arthur van Roermund, Andrea Baschiroto, 2011-09-15 Analog Circuit Design contains the contribution of 18 tutorials of the 20th workshop on Advances in Analog Circuit Design Each part discusses a specific to date topic on new and valuable design ideas in the area of analog circuit design Each part is presented by six experts in that field and state of the art information is shared and overviewed This book is number 20 in this successful series of Analog Circuit Design providing valuable information and excellent overviews of Topic 1 Low Voltage Low Power chairman Andrea Baschiroto Topic 2 Short Range Wireless Front Ends chairman Arthur van Roermund Topic 3 Power Management and DC DC chairman Michiel Steyaert Analog Circuit Design is an essential reference source for analog circuit designers and researchers wishing to keep abreast with the latest development in the field The tutorial coverage also makes it suitable for use in an advanced design course

Nanometer Variation-Tolerant SRAM Mohamed Abu Rahma, Mohab Anis, 2012-09-26 Variability is one of the most challenging obstacles for IC design in the nanometer regime In nanometer technologies SRAM show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density With the drastic increase in memory densities lower supply voltages and higher variations statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power This book is an invaluable

reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies Provides comprehensive review of state of the art variation tolerant SRAM circuit techniques Discusses Impact of device related process variations and how they affect circuit and system performance from a design point of view Helps designers optimize memory yield with practical statistical design methodologies and yield estimation techniques *Integrated Circuit and System Design*, 2004 **IEEE Transactions on Circuits and Systems**, 2006 Digital Integrated Circuits Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolić, 2008 **Energy Scalable Analog-to-digital Conversion Using Passive Sigma-delta Modulators** Jeffrey Loo, 2007 **A Power/area Optimal Approach to VLSI Signal Processing** Dejan Marko Marković, 2006 *Defect and Fault Tolerance in VLSI Systems* Robert Aitken, 2004 DFT 2004 showcases the latest research results in the in the field of defect and fault tolerance in VLSI systems Its papers cover yield defect and fault tolerance error correction and circuit system reliability and dependability

Approaches and Designs of Dynamic Voltage and Frequency Scaling Wayne Hung Cheng, 2007 **Pipelined Datapaths for AC Power Supplies** Jeffrey D. Siebert, 2005 **Leakage Power Analysis and Optimization in Deep-Submicron Technologies Under Process Variation** Saumil S. Shah, 2007 Circuit and Microarchitectural Techniques for Processor On-chip Cache Leakage Power Reduction Nam Sung Kim, 2004 *Digital Integrated Circuits* Jan M. Rabaey, 1996 Beginning with discussions on the operation of electronic devices and analysis of the nucleus of digital design the text addresses the impact of interconnect design for low power issues in timing and clocking design methodologies and the effect of design automation on the digital design perspective

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